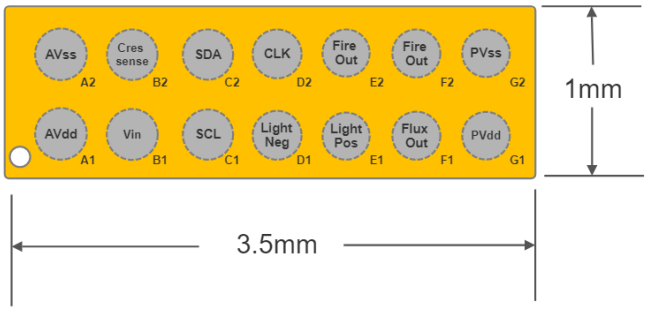
SL2001A Final Datasheet

Features

- Flexible architecture can provide laser FWHM pulses less than 2ns
- Dual Drive Outputs Support Peak Power up to 1000W
- High charging efficiency from a 2.8V to 24V supply
- Integrates needed blocks for Charging and Firing Resonant Mode Diode Lasers utilizing either EEL Diodes or VCSEL Arrays
- Integrated GaN/MOS Drive for Charging a Resonant Capacitor
- Inductor Current Control offers precise Resonant Capacitor Energy even with Input Voltage Fluctuations
- < 5 mW System No Load Power Consumption
- Up to 10 MHz Rep Rate limited by temperature rise in laser and other board components
- Dual Polarity LIGHT Output signal to indicate when laser fires with extremely low jitter (time error jitter < 0.1ns)
- Minimal external components enable extremely integrated and efficient layout
- Integrated I^2C interface for Output Power Control and Fault monitoring
- 7 MTP Bytes (3 time programmable) for fault and timing settings
- 219 OTP Bytes for customer usage
- 1 mm x 3.5 mm WLCSP Package

Product Description

The SL2001 is an Integrated Laser drive system including resonant capacitor charge control, timing control, laser safety monitoring and driver for Laser Time-of-Flight Measurement Systems employing Edge Emitting Laser Diodes or VCSEL Arrays.
The integrated Pulse Timing Controller uses a proprietary Architecture to provide Light pulses less than 3 ns wide with over 1000 watts of peak output power. An internal driver provides enough drive current to fire dual GaN/MOS FETs. An output trigger signal is provided for accurate start indication of Time-of-Flight measurements.
The Resonant Capacitor $\mathbf{C_{res}}$ is charged during each pulse cycle from an internal boost charger. This architecture implements an inductive current generator which charges $\mathbf{C_{res}}$ each cycle, and minimizes losses normally associated with transferring charge from standard High Voltage Supply Rails. The supply voltage for the charger can be as low as 2.8 volts and still achieve laser diode anode voltages of > 100 volts.
I^2C addressable registers and Multiple Time Programmable fuses are provided for light power adjustment and device monitoring/protection features.
The Laser Cathode is sensed to provide Laser Eye Safety.



Applications

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Range Finding
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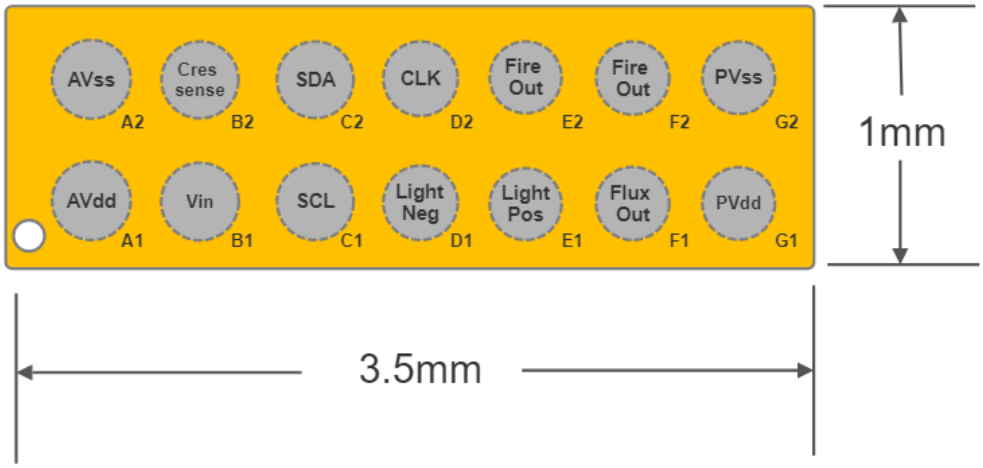

Figure 1: SL2001, 14 ball WCSP (0.5mm ball pitch) – Device Top View (bumps down)

Pin Definitions

Pin #	Name	Voltage Category (Vdc)	Description
A1	AV_{dd}	LV: (5V)	Analog supply for inputs
A2	AV_{ss}	LV (0)	analog ground for inputs
B1	V_{IN}	MV (24V)	inductor input voltage sense point
B2	CresSNS	LV (5V)	Cres voltage sense via external impedance
C1	SCL	LV (5V)	I^2C clock pin
C2	SDA	Output LV	I^2C data pin
D1	LightNeg	Output LV	Output indicating Laser Firing. low on rising edge of FireOUT and stays low for 75ns or until FireOUT goes low
D2	CLK	LV (5V)	Dual function timing input for capacitor charge and laser firing (see *Figure 4* and *Figure 5*)
E1	LightPos	Output LV	Output indicating Laser Firing. high on rising edge of FireOUT and stays high for 75ns or until FireOUT goes low
E2	FireOUT	Output LV	Output Drive for MOSFET or EGaN FET for External Cathode Clamp
F1	FluxOUT	Output LV	Output Drive for MOSFET or EGaN FET for External Cathode Clamp
F2	FireOUT	Output LV	2^{nd} FireOUT pin (shorted to pin E2) for lower board impedance to FET gate
G1	PV_{dd}	LV: (5V)	Power Supply for gate drive outputs
G2	PV_{ss}	LV (0)	Power Resonant Supply Voltage Rail Return for gate drive outputs

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Functional Block Diagram

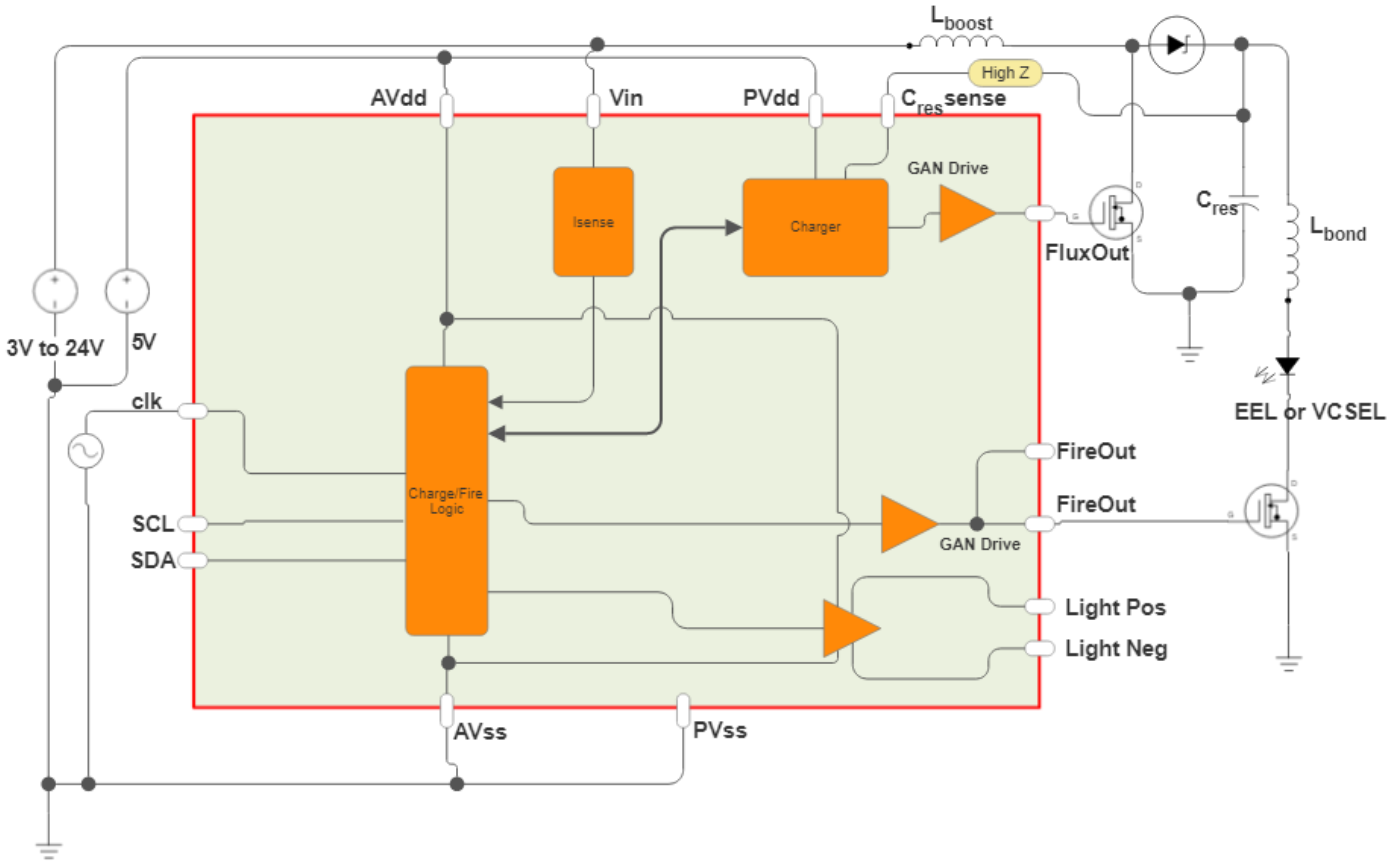


Figure 2: Functional Block Diagram

Absolute Maximum Ratings Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Max.	Units
Pin Voltages - Inputs	CLK		-0.3	AVdd+0.3	V
	AV_{dd}		-0.3	6.5	
	AV_{ss}		-0.3	0.3	
	PV_{dd}		-0.3	6.5	
	PV_{ss}		-0.3	0.3	
	SCL, SDA		-0.3	AV_{dd}+0.3	
	Cres_SNS		-0.3	AV_{dd}+0.3	
	V_{IN}		-0.3	28	
Pin Voltages - Outputs	FireOUT		-0.3	6.5	
	LightPOS,LightNEG		-0.3	6.5	
	FluxOut		-0.3	6.5	
Storage Temperature	T_{STG}		-50	150	°C
Junction Temperature	T_J		-40	150	
Lead Temperature (3)	T_{LEAD}			260	
Electrostatic Discharge (ESD) Protection (2)	V_{ESD}	HBM, Human Body Model per ANSI/ESDA/JEDEC JS-001	-2000	2000	V
		Charged-device model (CDM), per JEDEC specification	-500	500	V

Notes:

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information Note 1

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient	$R_{\Theta JA}$	30	°C/W
Thermal Resistance Junction to Board	$R_{\Theta JB}$	12	

Notes:

1) Simulated on 2S2P JEDEC 51-7 board.

Recommended Operating Conditions Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Vdd Supply Input Voltage	V_{Vdd}		4.5	5	6.0	V
V_{IN} Voltage	V_{IN}		2.7		24	V
AV_{dd} Bypass Capacitor	C_{AVdd}		-	0.1	-	µF
PV_{dd} Bypass Capacitor	C_{PVdd}		-	10	-	µF
V_{IN} Bypass Capacitor	C_{Vin}		-	22	-	µF
Operating Junction Temperature	T_J		-40		125	°C

Notes:

1) Device electrical characteristics are not guaranteed outside the recommended operating conditions.
2) Note that many electrical characteristics are specified for 4.5V < Vdd < 5.5V

Electrical Characteristics

(Unless otherwise specified, 4.5V < AV_{DD} < 5.5V, AV_{DD} = PV_{DD}, TJ = -40 °C to 125 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Current (Vdd)						
Input Supply Current, No Load	$I_{VddNL)}$	Laser fire freq < 1kHz, DAC codes 150	-	1.0	-	mA
Input Supply Current, Pulsing	$I_{Vdd(SW)}$	Laser fire freq = 250kHz, Fire Out cap = 100pF	-	3	-	mA
FireOut Drive Output – the two FireOut bumps are shorted on die						
FireOut Resistance Pull Down	$R_{DSL\_FireOut}$	$I_{OL\_FireOut}$ = 100mA			180	mΩ
FireOut Resistance Pull Up	$R_{DSH\_FireOut}$	$I_{OH\_FireOut}$ = 100mA			250	mΩ
Peak Sink Current	$I_{OL\_FireOut}$	$V_{OL\_FireOut}$ = 5V[1]		12	-	A
Peak Source Current	$I_{OH\_FireOut}$	$V_{OH\_FireOut}$ = 0V[1]		10		A
FluxOut Output						
FluxOut Resistance Pull Down	$R_{DSL\_FluxOut}$	$I_{OL\_FluxOut}$ = 100mA			720	mΩ
FluxOut Resistance Pull Up	$R_{DSH\_FluxOut}$	$I_{OH\_FluxOut}$ = 100mA			1	Ω
Peak Sink Current	$I_{OL\_FluxOut}$	$V_{OL\_FluxOut}$ = 5V[1]		3	-	A
Peak Source Current	$I_{OH\_FluxOut}$	$V_{OH\_FluxOut}$ = 0V[1]		2.5		A
LIGHT Drive Output – same parameters for LightPOS & LightNEG pins						
LIGHT Resistance Pull Down	R_{DSL_LIGHT}	I_{OL_LIGHT} = 100mA			1.44	Ω
LIGHT Resistance Pull Up	R_{DSH_LIGHT}	I_{OH_LIGHT} = 100mA			2	Ω
Peak Sink Current	I_{OL_LIGHT}	V_{OL_LIGHT} = 5V[1]		1.5	-	A
Peak Source Current	I_{OH_LIGHT}	V_{OH_LIGHT} = 0V[1]		1.25		A
FireOut Switching Parameters						
Maximum Switching Frequency (1)	f_{SW_MAX}	Note 1			10	MHz
Minimum On Time	TON_{MAX}	Minimum on time of the FireOut FET gate driver[1]	1			ns
LightPos & LightNeg output parameters						
Delay from FireOut rise to LightPos rise or LightNeg Fall		crossing threshold through 50% of Vdd[1]	-1		1	ns
FireOut to LIGHT rise cycle to cycle jitter		crossing threshold through 50% of Vdd with 100pF load on FireOUT & 10pF load on LightPos/Neg[1,2]	-100		100	ps
LightPos high & LightNeg low pulse width		crossing threshold (AV_{dd} – Avss) / 2	35		105	ns
Input Signal Parameters						
CresSNS resistance to AVss		While operating; forced to 0.2V		22		kΩ
CLK input rising threshold			1.7		2.6	V
CLK input falling threshold			1.1		1.8	V
CLK input voltage hysteresis			0.5		1	V
SDA/SCL input rising threshold					1.7	V
SDA/SCL input falling threshold			0.45			V
I^2C SCL Frequency					1	MHz
Timing Parameters						
CLK high to FluxOUT		CLK >50% to FluxOUT > 50%		5		ns

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FluxOUT PW range from FluxOUT>50% to FluxOUT<50%		typ values for range, see Basic Timing Description Section explanation [1]	5		2800	ns
FluxOUT PW Accuracy from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, V_{IN} =5V	188	200	212	ns
FluxOUT PW jitter from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, V_{IN} =5V[1,2]	-1		+1	%
CLK high to FluxOUT jitter from Clock>50% to FluxOUT>50%		DAC code h'A8 on Flux Time Reg cycle to cycle jitter; 100pF on FluxOUT[1,2]	-2.5		+2.5	ns
FluxOUT rise time		20% to 80% of PV_{dd} 100pF on FluxOUT[1,2]		0.45		ns
FluxOUT fall time		80% to 20% of PV_{dd} 100pF on FluxOUT[1,2]		0.45		ns
FluxOut Low to FireOut High range from FluxOUT<50% to FireOUT>50%		typ values for range, see Basic Timing Description Section explanation [1,3]	10		2800	ns
FluxOut Low to FireOut High Accuracy from FluxOUT<50% to FireOUT>50%		DAC code h'A7 on Charge Time Reg 100pF on FluxOUT & FireOUT[3]		200		ns
CLK low to FireOut		CLK <50% to FireOUT > 50%[1]		20		ns
FireOut PW range from FireOUT>50% to FireOUT<50%		typ values for range, see Basic Timing Description Section explanation [1]	1		320	ns
FireOut PW Accuracy from FireOUT>50% to FireOUT<50%		DAC code h'80 on Fire Time Reg, 100pF on FireOUT, VDD=5V, T=25C[1]	4.25	5	5.75	ns
FireOut PW jitter from FireOUT>50% to FireOUT<50%		DAC code h'7C on Fire Time Reg 100pF on FireOUT[1,2]	-4		+4	%
CLK low to FireOut jitter from Clk<50% to FireOUT>50%		DAC code h'7C on Fire Time Reg cycle to cycle jitter; 100pF on FireOUT[1,2]	-5		+5	ns
Supply Voltage Threshold and Fault Protection Parameters						
AV_{dd} & PV_{dd} rising threshold (selectable via Register 0x13 bits 7:6)		0x13 bits 7:6 set to 00	4.13	4.3	4.5	V
		0x13 bits 7:6 set to 01	2.4	2.5	2.6	V
		0x13 bits 7:6 set to 10	2.65	2.8	2.95	V
		0x13 bits 7:6 set to 11	4.6	4.8	5	V
AV_{dd} & PV_{dd} falling threshold (selectable via Register 0x13 bits 7:6)		0x13 bits 7:6 set to 00	3.9	4.05	4.2	V
		0x13 bits 7:6 set to 01	2.15	2.3	2.45	V
		0x13 bits 7:6 set to 10	2.45	2.6	2.75	V
		0x13 bits 7:6 set to 11	4.3	4.5	4.7	V
AV_{dd} & PV_{dd} Vth Hysteresis				0.26		V
delay from Vdd rising threshold to laser firing enabled		Note 1			1	ms
V_{IN} Over Voltage accuracy		threshold setting programmable per Table 7	- 7.5		7.5	%
Vin Under Voltage accuracy		threshold setting programmable per Table 6	- 7.5		7.5	%
Thermal Shutdown (OTP)	T_{SD}	Note 1	125			°C
Thermal Shutdown Hysteresis	T_{HYS}	Note 1		20		°C
Cres pre–Charge OV		Typical threshold setting programmable per **Error! Reference source not found.**8	-15		+15	%
Cres post Charge OV		Typical threshold setting programmable per **Error! Reference source not found.**8	-15		+15	%
Cres pre-charge UV		V_{IN} = 5V, Rsns=6.8MΩ, Vth code 0 per Table 8	-0.265	V_{IN} -0.12	+0.265	V
		V_{IN} = 5V, Rsns=6.8MΩ, Vth code 1 per Table 8	-0.215	V_{IN} -1	+0.215	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		V_{IN} = 5V, Rsns=6.8MΩ, Vth code 2 per Table 8	-0.215	V_{IN} -1.3	+0.215	V
		V_{IN} = 5V, Rsns=6.8MΩ, Vth code 3 per Table 8	-0.215	V_{IN} -2.2	+0.215	V
Cres post-charge UV		Typical threshold setting programmable per **Error! Reference source not found.**8	-25		+25	%

Notes:

1) Guaranteed by design and characterization, not production tested
2) cycle to cycle jitter is specified for no change in any environmental conditions. It shows a Gaussian distribution with 3 sigma numbers specified as limits
3) Only valid for operating mode where CLK falling edge does NOT trigger the laser to fire.

Overview

The SL2001 is a fully integrated Resonant Mode Controller for Driving EEL or VCSEL Laser Diodes. It uses a current source to provide a predetermined amount of charge to the laser resonant capacitor each cycle from a low input voltage source allowing the resonant capacitor voltage to increase as a function of the amount of charge. It is possible to achieve high resonant capacitor voltage from a relatively low input **V_{IN}**. The small Resonant Capacitor values which match the small predicted parasitic inductance values can be used without need for a high voltage input rail. This eliminates the need for a boost converter to provide the needed high Resonant Capacitor Voltage. A series inductor is used to provide the current to charge the Resonant Capacitor to the needed voltage for the Laser Diode resonant circuit. The stored energy in the Resonant Capacitor is then transferred to the Laser Diode during the “Firing” phase. The SL2001 monitors the input Voltage (**V_{IN}**) and adjusts the amount of time the input inductor is “fluxing” to compensate for variations in **V_{IN}**. Fault trigger levels can be set for **V_{IN}** undervoltage and overvoltage. The SL2001 also monitors the voltage on the Resonant Capacitor (**C_{res}**) for under and over voltage conditions. These Fault trigger points are set via internal registers and programmed over the I^2C interface. A description of the Fault detection and operation is shown in the section *Protection and Fault Information*Figure 17: SL2001 Fault Diagram. High current drive for either MOS or GaN FETs is also integrated as well as indicators for light pulse start. The device can also detect and shunt current away from the laser if the firing FET fails for Eye Safety.

Detailed Pin Descriptions

Pins A1: AV_{dd} and A2: AV_{ss}

AV_{ss} is the Main ground return for the analog circuitry and the Light output signals. This circuitry is supplied by **AV_{dd}**, a decoupling capacitor between **AV_{dd}** and **AV_{ss}** should be placed as close as possible to the IC. **AV_{ss}** should nominally be tied to board ground within a few millimeters of the SL2001 in a board location that is outside of the current path between the ground input to the board and the ground of the resonant capacitors. Special attention should be paid to preventing switching noise between **AV_{ss}** and the ground pins of the chip that is receiving the **LightPos** and **LightNeg** output signals.

Pins G1: PV_{dd} and G2: PV_{ss}

PV_{ss} is the main power ground return for the gate drive circuitry. The gate drive circuitry is supplied by **PV_{dd}**. A decoupling capacitor between **PV_{dd}** and **PV_{ss}** should be placed as close as possible to the IC. **PV_{ss}** should be tied to the power ground plane in a manner to minimize inductive voltage ringing between the GaN FET used for laser firing (1^{st} priority) as well as minimize the inductive voltage ringing between the GaN FET used for inductor current ramp (2^{nd} priority).

Pin B1: V_{IN}

This pin is used to sense the inductor input voltage for Fault recognition as well as to maintain a constant inductor peak current. The V_{IN} over voltage and under voltage Fault Thresholds are set via register 0X13.

Pin B2: CresSNS

The **CresSNS** pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in *Figure 18* for sensing at the laser anode and in *Figure 19* for sensing of the laser cathode. The fault threshold voltage options for 6.2MΩ or 6.8MΩ resistor values are shown in *Table 9.* External resistor values between 5MΩ and 8MΩ are valid and will change the Cres fault threshold values shown in the *Electrical Characteristics section* per the equation below.

$$Cres\ Fault\ Thresold = Fault\ Threshold\ with\ 6.8M\Omega * \frac{External\ Rcres\ value}{6.8M\Omega}$$ *Equation 1:*

Please ensure that the external resistor can support the maximum voltage on the C_{res} net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2001 takes when a fault is detected is described in ***Error! Reference source not found.***.

Pins C1: SCL and C2: SDA

These are the Clock and Data pins for I²C interface. The I²C Interface is always accessible. High level register descriptions are shown in *Table 3***Error! Reference source not found.**. Four selectable I²C addresses are available for the SL2001. These are selected by changing bits 1 & 0 in register address 0x16, explained in *Table 1*. These bits can be changed via an I²C command, in which case the address will change immediately such that all subsequent I²C communication will use the new address. The address bits can also be loaded into the 3-time programmable MTP such that the I²C address option will always be loaded at part start-up.

Register 0x16 bit1 bit0	I²C Address
00	0001001x
01	0101001x
10	1001001x
11	1101001x

Table 1: I²C Startup Addresses

Pins D1: LightNeg and E1: LightPos

These pins provide an indication of the **FireOUT** signal going high with an extremely small amount of signal jitter from period to period (3 sigma jitter <100ps).

Pin D2: CLK

This multi-function pin supplies the main clock to the pulse timing generator. The rising and falling edges of the clock can be programmed to trigger the gate drive outputs in 2 different modes as described in the timing control section below in *Figure 3: Mode1 Timing* and *Figure 4.*

Pins E2 and F2: FireOUT

These pins provide an extremely fast gate drive signal with adjustable pulse width between 0.5ns and 100ns for the GaN or MOS Gate Drive. Two adjacent pins are used to reduce the parasitic inductance on the die and on the board.

Pin F1: FluxOUT

This pin provides a fast gate drive signal with adjustable pulse width between 5ns and 1µs for the GaN FET that is used to ramp current in the inductor and charge the resonant capacitor.

Timing Description: Inductor Flux, C_{res} Charge and Laser Fire

Mode1 Timing Steps

The **CLK** rising edge triggers **FluxOUT** to rise, starting the Flux time (inductor current ramp). The Flux time "Tflux(ns)" is controlled by register 0x10 with 2.5% steps from 5ns to 2.8µs as shown in *Figure 8: Flux Time vs. DAC Code*. The falling edge of the **FluxOUT** signal starts the **C_{res}** Charge time. The Charge time "Tcharge(ns)" is controlled by register 0x11 with 2.5% steps from 10ns to 2.8µs as shown in *Figure 12*. At the end of the Charge time, the **FireOUT** signal goes high to begin the Fire time. The Fire time "Tfire(ns)" is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in **Error! Reference source not found.**.

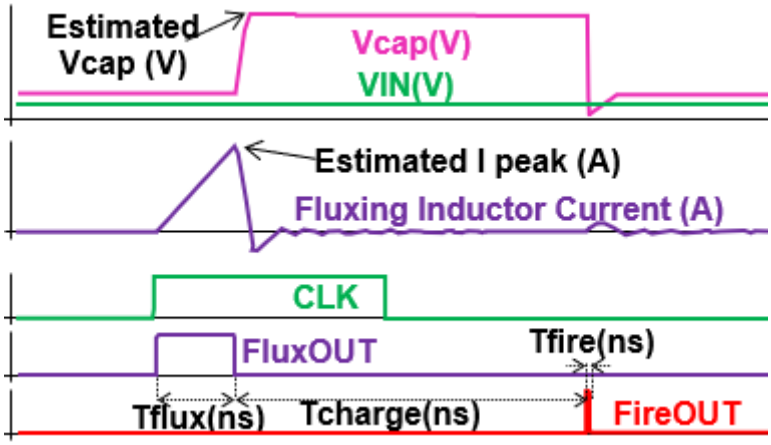


Figure 3: Mode1 Timing

Mode2 Timing Steps

The **CLK** rising edge triggers the **FluxOUT** signal to rise, starting the Flux time (inductor current ramp).The Flux time "Tflux(ns)" is controlled by register 0x10 with 2.5% steps from 5ns to 2.8µs as shown ***Error! Reference source not found.***.The Charge time "Tcharge(ns)" is controlled by the pulse width of the **CLK** input pin. At the falling edge of the **CLK** input pin, the **FireOUT** signal goes high to begin the Fire time. The Fire time "Tfire(ns)" is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in ***Error! Reference source not found.***.

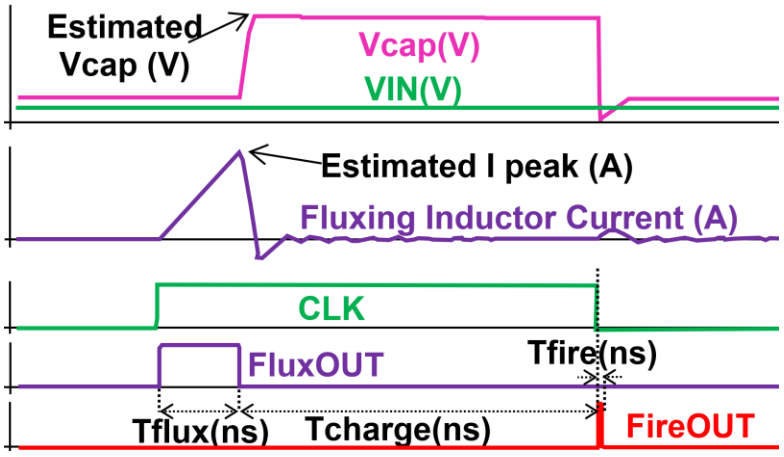


Figure 4: Mode2 Timing

The timing for Fluxing, Charging (mode1 only), and Firing is controlled by the circuit *in Figure 5**Error! Reference source not found.***. A current (I1) is set-up by forcing a voltage (Vref1) across a DAC programmable resistance value. That current (I1) is then mirrored to a current I2 and used to charge a capacitance to a voltage level (Vref2). When the **CLK** signal goes high, the **FluxOut** signal will go high until the capacitor is charged to the Vref2 level. The **FluxOut** high time will follow *Equation 2*.

$$\textit{Equation 2}: Fluxout\ high = \frac{C * Vref2 * Rdac}{Vref1 * Gmirror}$$

The **FluxOut** high time will change proportionally to a change in the DAC resistance value (Rdac). The **FluxOut** high time will change inversely proportional to a change in the voltage of Vref1 or the gain of the current mirror (Gmirror).

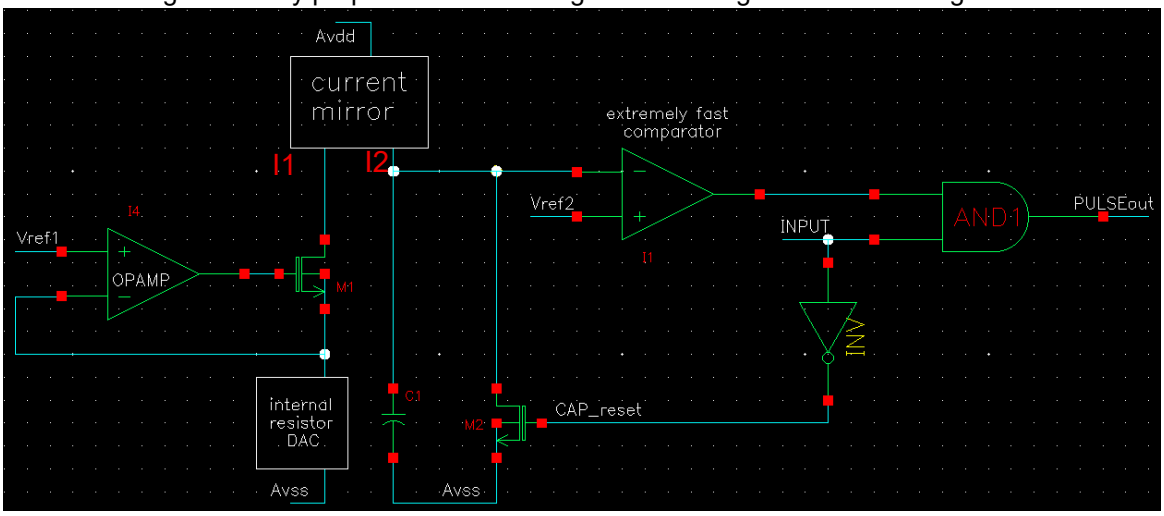


Figure 5: Flux Timing Generation

Three 8-bit registers (0x10h, 0x11h, 0x12h): FluxTime, ChargeTime and FireTime correspond to DACs for each of these timing parameters. Their resistor value increases by ~2.5% for each DAC step, with a minimum resistor value of 2kΩ and a maximum resistor value of 1.085MΩ with each resistor value set by *Equation 3* for Rdac codes from zero to 255.

$$\textit{Equation 3: } Rdac\ value = 2k * 1.025^{(Rdac\ code)}$$

The Rdac value changes linearly on a log scale as shown in the graph in ***Error! Reference source not found.***. Note that the Rdac code is an exponent in the equation above.

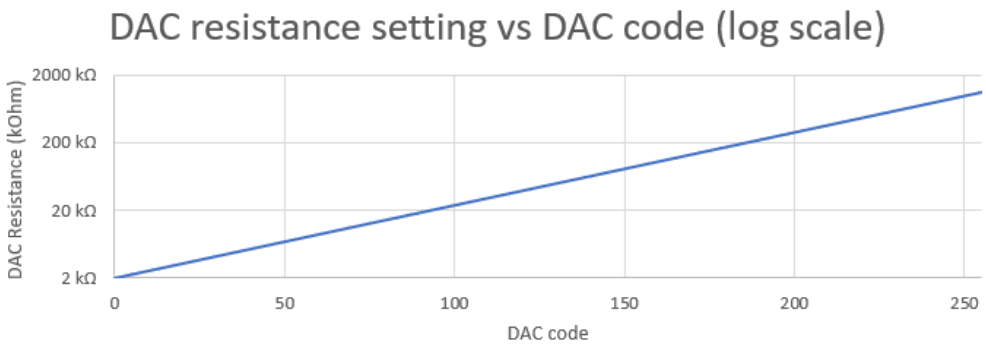


Figure 6: DAC Resistance Setting vs. Code

The Flux time setting can be set to vary inversely with the V_{IN} voltage or to be fixed and not change as V_{IN} changes. A brief explanation is included below for how the inversely proportional to V_{IN} mode can achieve a constant peak inductor current and near constant laser peak current level.

Flux Time Control and Cres Charge Control

The Schottky Anode Voltage Shown in *Figure 7* is pulled to Ground during the Fluxing time as shown in *Figure 2*. The voltage across the inductor with the Schottky Anode at ground is fixed to V_{IN} – 0V = V_{IN}. Using *Equation 4***Error! Reference source not found.** and knowing that the inductor current at the beginning of the Fluxing time is always zero, we can define the equation components as V= V_{IN}, L=inductor value dt=Fluxing time. By rearranging the equation, we can solve for the inductor current at the end of the Fluxing period.

Equation 4: $$i_L = \frac{V}{L}\int_0^{T_{flux}} dt$$

Equation 5: $$I_{Lpeak} = V_{in} * \frac{T_{flux}}{L}$$

The default setting for the fluxing time control of the SL2001 uses the equation above to maintain a constant peak inductor current at the end of the Fluxing time (IL_peak) by changing the Fluxing time inversely proportional to changes in the V_{in} voltage.

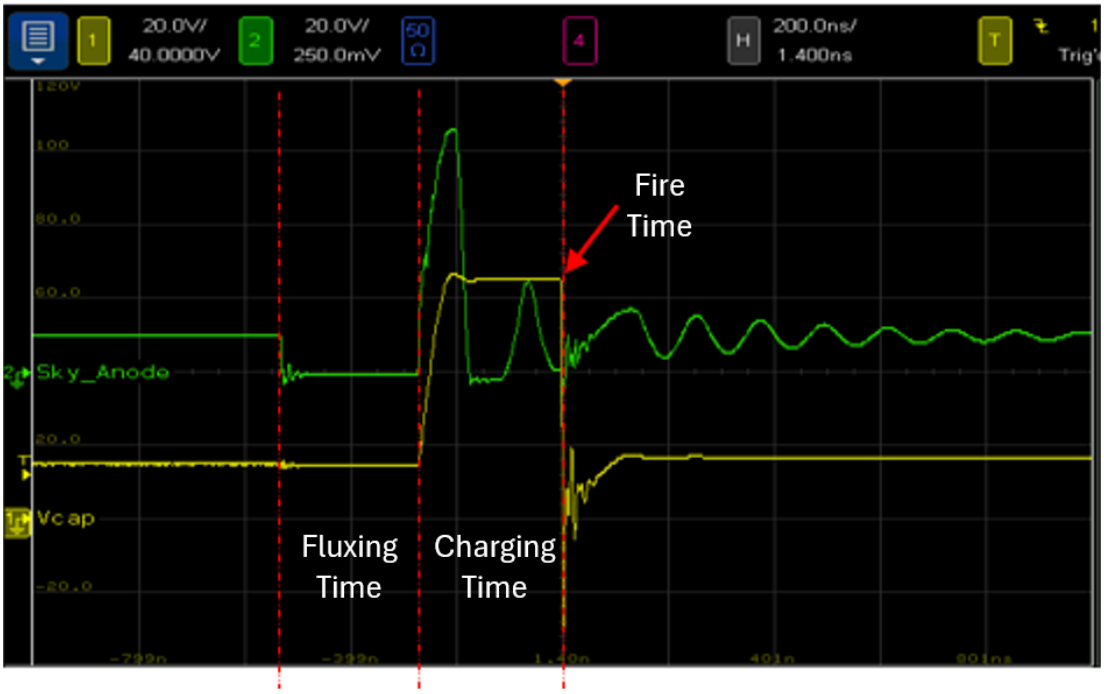


Figure 7: Firing Sequence

The V_{IN} dependent Flux time can be set for an average V_{IN} voltage of either 5V or 12V. The Flux time will automatically change inversely to V_{IN} over a V_{IN} range of 3.5V to 7.5V, or 8.4V to 18V depending upon the average V_{IN} setting of 5V or 12V. If V_{IN} strays beyond the range settings above (for example, >7.5V for V_{IN} dependent 5V setting), there is a risk that Flux time will no longer automatically change to correct for the changes in V_{IN} allowing the inductor current peak to also change in proportion to V_{IN}.

The graph below in *Figure 8 Figure 8: Flux Time vs. DAC Code*shows the behavior of the Flux Time to the V_{IN} voltage. The orange curve has longer Flux time due to the lower V_{IN} voltages (3.5V for the 5V setting and 8.4V for the 12V setting), while the red curve has a shorter Flux time due to the higher V_{IN} voltages (7.5V for the 5V setting and 18V for the 12V setting).

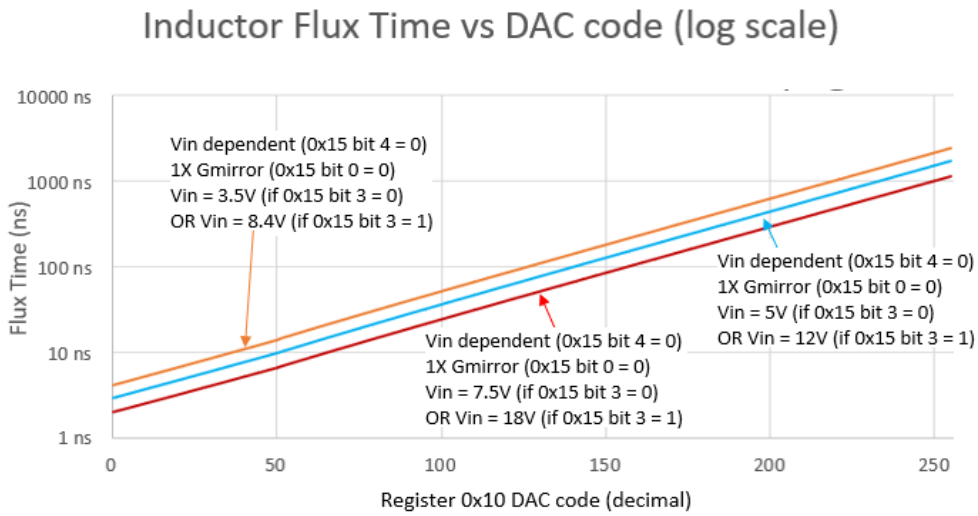


Figure 8: Flux Time vs. DAC Code (Vin Dependent)

The Flux time varies inversely with the V_{IN} voltage and as a result the peak inductor current (IL_peak) will be constant for a given value of inductance. Since Tflux in *Figure 8* is the same for the 5V & 12V settings, the IL_peak is higher for V_{IN} = 12V than for V_{IN} = 5V as predicted by *Equation 5* .

The graph in *Figure 9: Peak Current vs. DAC Code* below shows the Tflux with Gmirror=1 & 440nH inductor or Gmirror=2 & 220nH inductor.

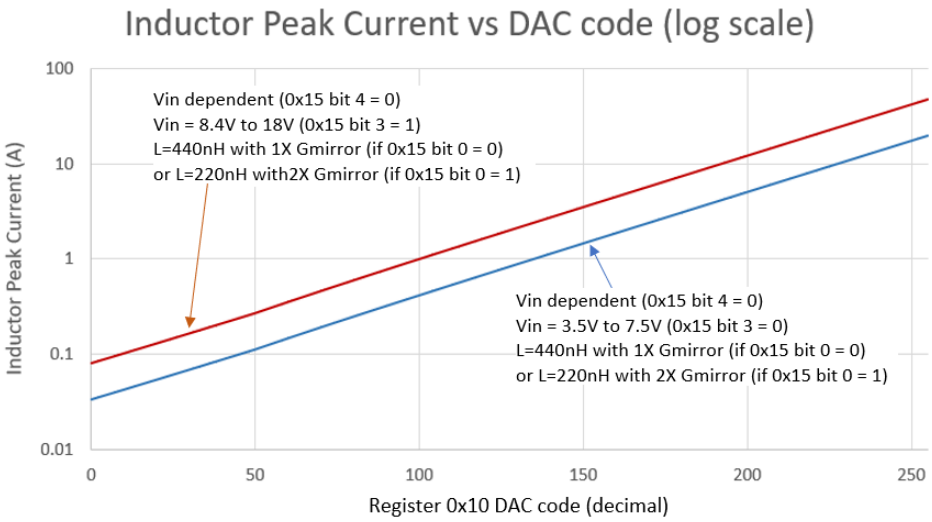


Figure 9: Peak Current vs. DAC Code (Vin Dependent)

For smaller values of inductors, a 2x Gmirror setting is available. This mode approximately doubles the current into the capacitor of which decreases Flux Time for a given DAC setting by a factor of ~1.8. Users can use the I^2C interface to adaptively change the DAC resistor setting which varies the Inductor Flux time (Tflux). This will change the inductor peak current (IL_peak) which in turn will increase or decrease the voltage of the resonant capacitor (Cres) and the current through the laser diode when it is fired. For customers who want to adaptively change the peak inductor current (IL_peak), but do not want to use the I^2C interface, an option is included where the part does not automatically vary the Flux time (Tflux) as V_{IN} varies. With this option, the customer can vary V_{IN} to change the inductor peak current (IL_peak) according to *Equation 5*.

The graph in *Figure 10* ***Error! Reference source not found.*** below shows the inductor flux time (Tflux) for the mode where the Flux time is independent of V_{in} for the 1x and 2x current mirror gain (G_{mirror}) settings.

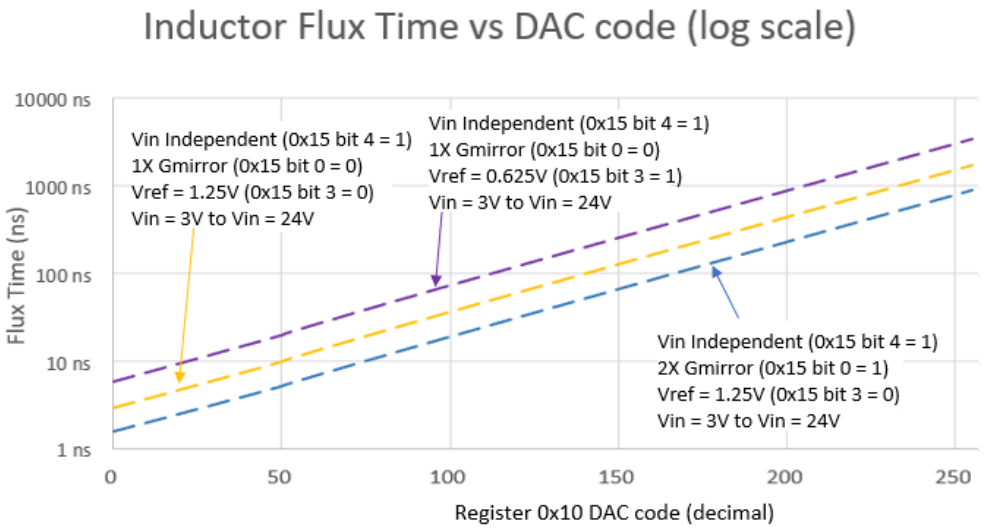


Figure 10: Flux Time Independent upon V_{IN}

The Flux time does not change as the V_{IN} voltage changes, the corresponding peak inductor current (IL_peak) will change for a given value of inductance per the Graph in *Figure 11*.***Error! Reference source not found.*** This graph shows the Flux Times at different values of V_{IN} with a G_{mirror}=1 and a 440nH inductor or G_{mirror}= 2 and a 220nH inductor.

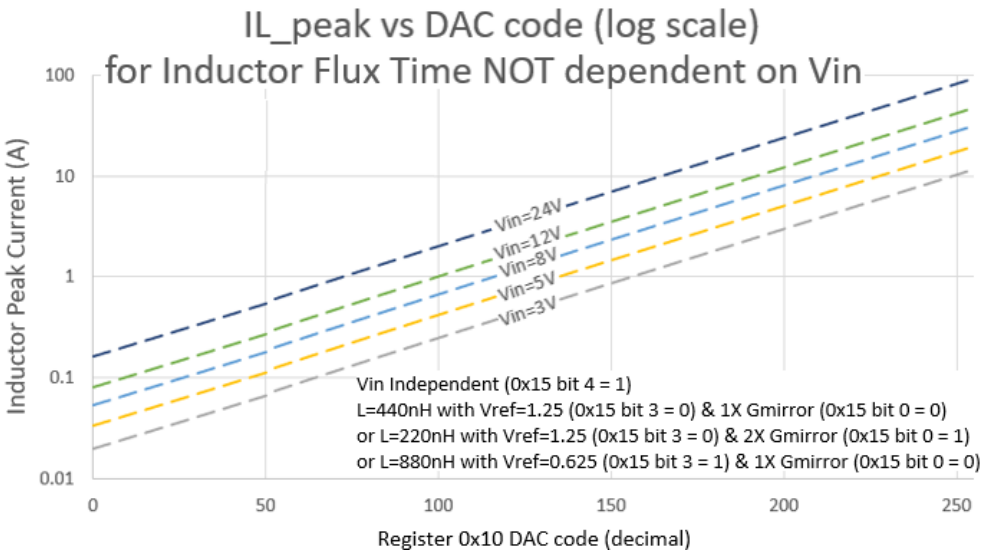


Figure 11: Peak Current Independent upon V_{IN}

For the Flux Time Dependent upon V_{IN} mode, the DAC range can be modified by selecting 1X or 2X Gmirror setting via Register 0x16 bit 0 as shown in Figures 8 and 9. For the Flux Time Independent upon V_{IN} mode, the DAC range can be modified by selecting Vref = 1.25V or 0.625V via Register 0x16 bit 3 and by selecting 1X or 2X Gmirror setting via Register 0x16 bit 0 as shown in *Table 2* and in Figures 10 and 11.

decimal code	00x15 bit3=0 00x15 bit0=1	00x15 bit3=0 00x15 bit0=0	00x15 bit3=1 00x15 bit0=0
fixed Flux DAC range	low L range, Vref = 1.25V and 2X Gmirror	middle L range, Vref = 1.25V and 1X Gmirror	high L range, Vref = 0.625V and 1X Gmirror

Table 2: Flux Inductor Ranges

For timing *Mode 1* described in *Figure 12*, the Charge Time (the time between the **C_{res}** voltage rising and the laser firing) is set with the same formula as the Flux time; however, each charge time will be ~4ns longer than the same code setting for Flux Time, Due to internal noise, the Charge time may vary during operation to as much as 25% below the set time range. This does not affect the peak light current from the laser. *Figure 12* below shows the Charge Time verses DAC code for Mode 1.

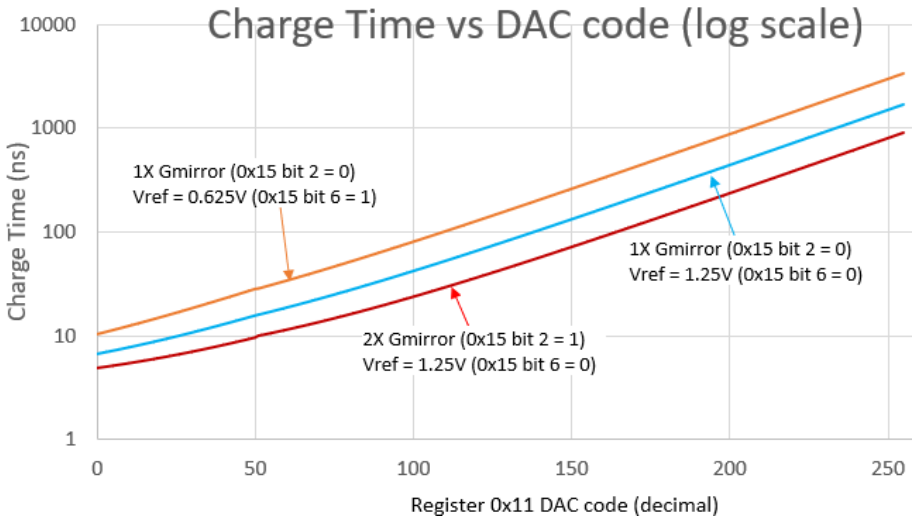


Figure 12: Charge Time verses Register 0x11 DAC code for Mode 1

For timing *Mode 2* described in below, the Charge Time is set via the duty cycle of the clock.
The Charge Time should be set high enough to cover the post charge blanking times for the Cres sense overvoltage and undervoltage circuitry, which is ~400ns. 1µs is a good typical setting since it is not long enough to get any noticeable voltage degradation in **C_{res}** after charging while also covering the **C_{res}** sense blanking times with sufficient margin.

The Pulse Width of the **FireOUT** signal can be adjusted to create a balance between the gate ON time to reach peak laser current, not violating the negative voltage constraints of the laser, and avoiding a 2nd pulse of light through the laser. *Figure 13* below shows the Fire Time verses DAC code for the 3 possible DAC modes.

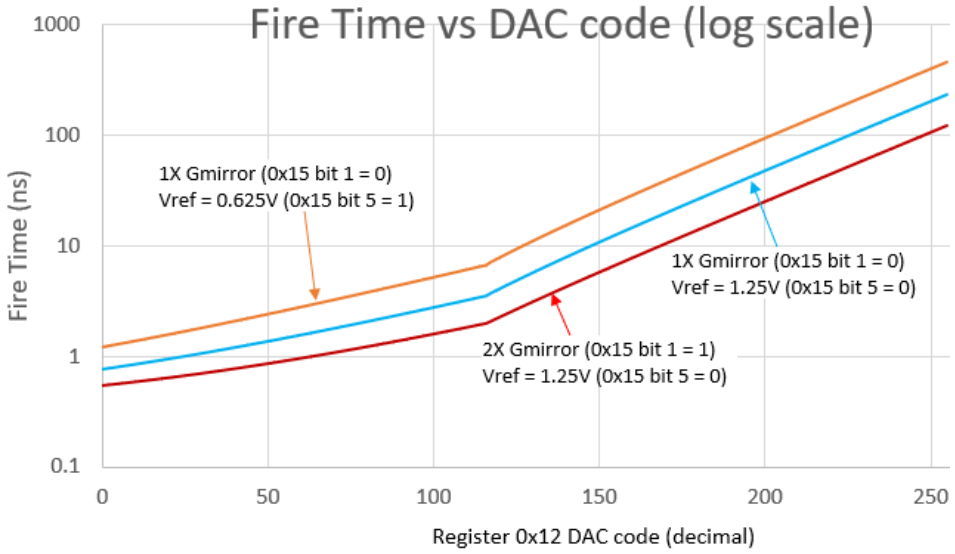


Figure 13: Fire Time verses Register 0x12 DAC code

High Level Register Map

A basic Register Map is shown below but for more detailed information please consult the SL2001 GUI Application Note.

Regmap	
read/write backed by MTP	Register Bytes 0x10 to 0x16 can be read/written from/to and are loaded during start-up by 3 times programmable MTP memory.
read/write I2C only	These register Bytes can be read and written to/from via I2C but they are not associated with any nonvolatile memory addresses
read only	These bits are set internally by the SL2001 and can ONLY be read via I2C (not associated with any nonvolatile memory addresses)
read/reset status	The SL2001 will set bits of register 0x90 to one if an associated fault occurs. The user can reset any of these bits back to zero viaI2C write (not associated with any nonvolatile memory addresses)
NVM action	Writing a one to bit one or zero of register 0x8A via I2C will cause the SL2001 to perform a write or read from the non volatile memory address in register 0x8B. After completing the requested action, the SL2001 will auto clear this bit back to a zero. (not associated with any nonvolatile memory addresses)

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0
Flux Time Control	0x10	FluxTime[7]	FluxTime[6]	FluxTime[5]	FluxTime[4]	FluxTime[3]	FluxTime[2]	FluxTime[1]	FluxTime[0]
Charge Time Cntrl	0x11	ChargeTime[7]	ChargeTime[6]	ChargeTime[5]	ChargeTime[4]	ChargeTime[3]	ChargeTime[2]	ChargeTime[1]	ChargeTime[0]
Fire Time Control	0x12	FireTime[7]	FireTime[6]	FireTime[5]	FireTime[4]	FireTime[3]	FireTime[2]	FireTime[1]	FireTime[0]
Function 3	0x13	SupplyOK_VTH[1]	SupplyOK_VTH[0]	VinOV_VTH[2]	VinOV_VTH[1]	VinOV_VTH[0]	DO NOT USE	VinUV_VTH[1]	VinUV_VTH[0]
Function 4	0x14	DutyCyleMode	FluxOV_VTH[1]	FluxOV_VTH[0]	FireOV_VTH[2]	FireOV_VTH[1]	FireOV_VTH[0]	FluxUV_VTH[1]	FluxUV_VTH[0]
Function 5	0x15	DigSoftRset	TChargeRef	TFireRef	TFluxRef[1]	TFluxRef[0]	TCharge2x	TFire2x	TFlux2x
Function 6	0x16	FluxOVBehavior[1]	FluxOVBehavior[0]	CresUVBehavior	FireUV_VTH[1]	FireUV_VTH[0]	DontSkip1stFlux	i2c_address[1]	i2c_address[0]
nvm_ctrl	0x8A	vpp_mode	keep these 3 bits at 000			vpp_req	wr_en	wr	rd
nvm_addr	0x8B	nvm_addr[7:0]							
nvm_wdata	0x8C	nvm_wdata[7:0]							
nvm_rdata	0x8D	nvm_rdata[7:0]							
status_fault	0x90	Over Temp	VinOV	VinUV	CresUV pre-Charge	CresOV pre Charge	CresOV post Charge	CresUV post Charge	SupplyOK Fault

Table 3: Register Map

Non Volatile Memory (NVM)

In addition to real time I²C programmability during operation, registers 0x10 though 0x16 above can also be set via SL2001's three-time programmable Multiple Time Programmable (MTP) ROM, which will be loaded to those registers when the part starts-up. SL2001 also contains 219 additional One Time Programmable (OTP) Bytes in memory addresses (0x17-0x5F and 0x67-0xAF and 0xB7- 0xFF) that users can use as they wish. These are additional Bytes of memory that have no direct impact on product operation and can be loaded with any information, for example board or laser specific information that a microcontroller could use to modify register settings during operation due to temperature or other variations.

One example for use of the 219 Bytes of OTP would be to store board specific information about the optimal Flux Time Control (Register 0x10) codes for various laser temperatures and/or other environmental variants to achieve one or several desired Light power profiles. During operation, the temperature could then be sensed near to the laser, and the code could then be read back via I²C for the memory address associated with that temperature, such that the code in that memory address could then be written via I²C to register 0x10 to modify the Flux Timing.

Protection and Fault information

The SL2001 offers several highly programmable fault options and settings. A brief summary of the Fault Options with more specific information about each option is described in this section.

Hiccup Mode (Default):

When a Fault is registered in the Digital circuitry, the SL2001 will stop immediately and set both the **FluxOUT** and **FireOUT** pins to low (zero V) for 28ms. After 28ms, the SL2001 will check whether the fault is still present. If the fault is still present, the SL2001 will continue holding both **FluxOUT** and **FireOUT** low and wait another 28ms before checking the fault status again. Once the fault is no longer present (checking every 28ms), the SL2001 will immediately begin driving both the **FluxOUT** and **FireOUT** pins again per the previous clock and timing settings.

Mask Faults:

The SL2001 can be programmed via I²C to mask or react to any of the faults.

Fault Latch Off Mode:

The SL2001 has the option over the I²C interface to not "hiccup" but rather to "latch off" when any of the selected faults are registered. If the SL2001 does latch-off due to a fault, then the **FluxOUT** and **FireOUT** pins will be held low until either 1 of the 2 events occurs:

1. The DigSoftReset bit (bit 7 of register 0X15) is set to a 1 via the I²C interface (this bit will be reset back to 0 automatically upon reset)
2. The **AV_{dd}** voltage is brought below 1V, then brought back up above 3V

Upon either event 1 or 2 occurring, the SL2001 registers will go through its start-up sequence such that all registers will be set according to the NVM settings and then check whether any faults exist before beginning to drive the **FluxOUT** and **FireOUT** pins again.

Fault Behavior During Device Start-up

The SL2001 Fault operation follows the sequence shown in *Figure 14*.

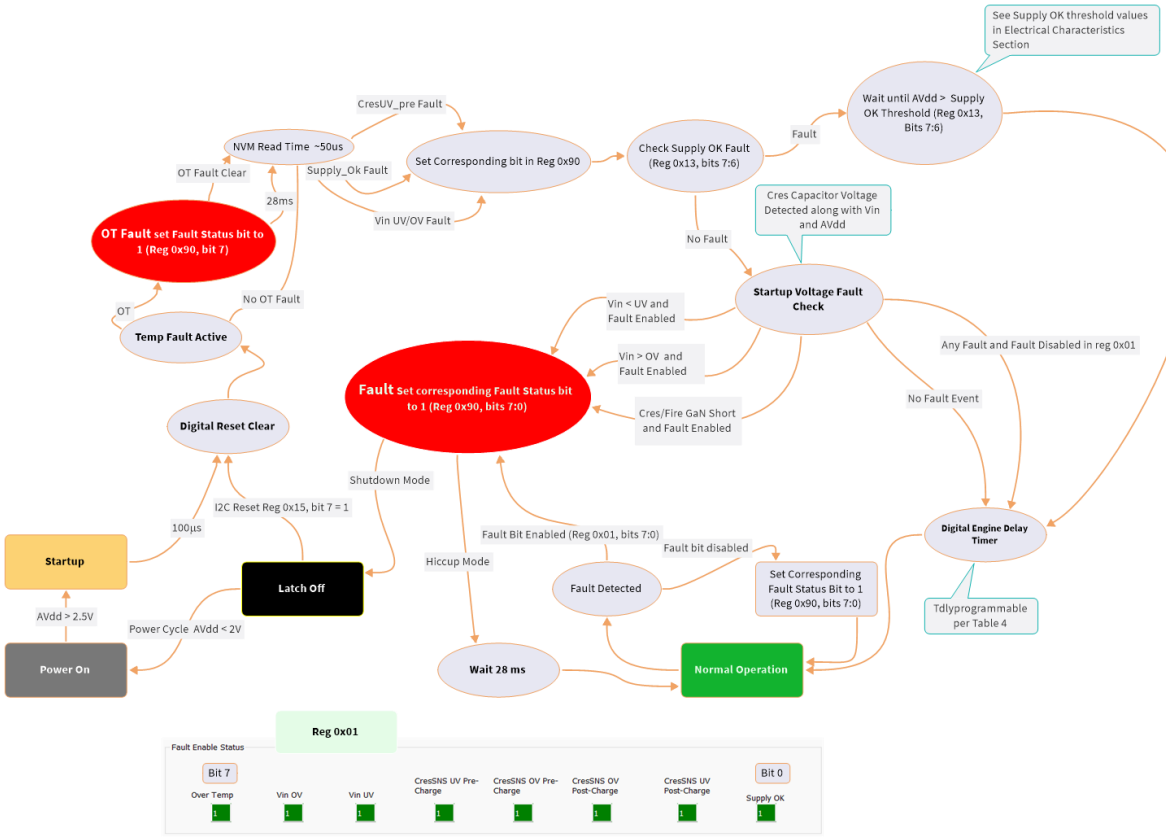


Figure 14: State Diagram of Operation and Fault Behavior

Starting from the bottom left corner of *Figure 14:* upon $\mathbf{A_{Vdd}}$ rising above a voltage of approximately 2.5V, the part will wait approximately 100µs and then clear the reset for the internal Digital Engine and begin the startup fault checking.

The first fault to be checked is over temperature protection, which has a typical rising threshold of approximately 140C. Per the Electrical Characteristics section, the rising threshold will always be higher than 125C and the falling threshold will be approximately 20C below the rising threshold. If an over temperature protection fault is triggered, the SL2001 will wait until either the fault is no longer triggered or 28ms has passed, then continue through the rest of the startup sequence. After waiting approximately 50µs, the CresUV_pre, Supply OK and V_{IN} UV/OV faults will all be checked. If any of the CresUV_pre or V_{IN} UV/OV faults are present, their corresponding bit in the Fault Status Register (0x90) will be set to 1, then (only if the corresponding Fault Enable bit in Register 0x01 is set to 1 and the Supply OK Fault is not present) the SL2001 will immediately move to FAULT mode. If the Supply OK Fault is present, SL2001 will wait until the Supply OK Fault is no longer present, then proceed to normal operation (after a programmable delay time). In normal operation, all Faults will be continuously monitored. If any Fault occurs, its corresponding bit in the Fault Status Register (0x90) will be set to 1, then (only if that Fault's corresponding bit in the Fault Enable Register 0x01 is set to 1) the SL2001 will enter FAULT mode. If the SL2001 enters fault mode and Hiccup Mode is selected for the fault that has occurred (Register 0x02 corresponding bit is set to 0), then the SL2001 will hold the FluxOUT and FireOUT pins low, wait for approximately 28ms, and re-enter Normal Operation. If the SL2001 enters fault mode and Shutdown Mode is selected for the fault that has occurred (Register 0x02 corresponding bit is set to 1), then the SL2001 will enter Latch Off mode where the FluxOUT and FireOUT pins will be held low. The SL2001 can be restarted from Latch Off mode by either bringing AVdd below approximately 2V or by writing the DigSoftReset bit to 1 (Reg 0x15 bit 7).
In *Figure 14*, the Digital Reset Clear state that is entered immediately after Startup or upon exit from Latch Off will reset all bits of the Fault Status Register (0x90) to 0. For all other times during operation, the Fault Status Register bits

are “sticky”, meaning that if any bit is set to 1 due to its corresponding fault occurring, then it will stay as a 1 unless the user changes it back to a 0 via an I2C write.

To avoid getting a SupplyOK fault flag in the Fault Status register (0x90) during startup, the AV_{dd} slew rate needs to be fast enough so that after AV_{dd} crosses 2.5V, within 100us, AV_{dd} will reach 4.5V. The slew rate to prevent a SupplyOK fault flag can be set by *Equation 6* below:

Equation 6: $AVdd\ Slew\ rate\ > \frac{4.5V-2.5V}{100\mu s} = \frac{2V}{100\mu s}$

If a V_{IN} UV Fault occurs and is enabled (Register 0x01 bit 5 set to 1), the SL2001 will enter FAULT mode and either Hiccup (wait 28ms to enter Normal Operation) or Latch Off. To avoid the this from happening during startup, 3 options are available:

1) the V_{IN} UV Fault can be disabled via non volatile memory (set Register 0x01 bit 5 to 0)
2) the V_{IN} supply can be ramped above the V_{IN} UV threshold voltage before the AV_{dd} supply starts ramping from zero Volts
3) **Error! Reference source not found.**below can be met

Equation 7: $V_{IN}\ slew\ rate\ to\ prevent\ UV\ during\ startup\ > \frac{Vin\ UV\ rising\ threshold}{\frac{2V}{SlewRate\_AVdd} + 150\mu s + Tdlyprogrammable}$

The V_{IN} UV rising threshold is programmable per *Table 4* and the Tdlyprogrammable time per *Table 5*.

For example, in order to meet with separate V_{IN} and AV_{dd} supplies starting to ramp from zero Volts at the same time with a Tdlyprogrammable setting of 888µs (Register 0x00 bits 5:4 = 11), AV_{dd} slew rate of 1V/ms and V_{IN} UV rising threshold of 9.1V (Register 0x13 bits 1:0 = 10), the V_{IN} slew rate would need to be greater than 9.1V / (2V/1000V/s + 150µs + 888µs) = 3 V/ms.

If V_{IN} and AV_{dd} are operated from the same supply, then the slew rate for V_{IN} and AV_{dd} are the same and *Equation 7* simplifies to *Equation 8* below:

Equation 8: $V_{IN}\ \&\ V_{DD}\ (from\ same\ supply)\ slew\ rate\ to\ prevent\ UV\ during\ startup\ > \frac{Vin\ UV\ rising\ threshold-2V}{150\mu s + Tdlyprogrammable}$

For example, in order to meet *Equation 8* with a single power supply driving both V_{IN} and AV_{dd} with a Tdlyprogrammable setting of 888µs (Register 0x00 bits 5:4 = 11) and V_{IN} UV rising threshold of 4V (Register 0x13 bits 1:0 = 01), the V_{IN} & AV_{dd} (from same supply) slew rate would need to be greater than (4V – 2V) / (150µs + 888µs) = 4 V/ms.

bit5	bit4	Register 0x00, bits 5:4, FuseTime
0	0	Tdlyprogrammable = 18us
0	1	Tdlyprogrammable = 89us
1	0	Tdlyprogrammable = 355us
1	1	Tdlyprogrammable = 888us

Table 5: Programmable delays for OTP read mode to full Function mode.

Waveforms for different startup examples are available in the section

Startup Fault Condition Examples

The **CresSNS UV_Precharge** comparator (see *Figure 15*) is active after OTP read is completed to detect a short circuit from the cathode of the laser to ground. The V_{IN} voltage should not rise higher than the laser light threshold until at least 200us after the AV_{dd} voltage is higher than 2.5V for this start-up short detection to trip immediately during start-up (before the laser light causes an eye safety concern**).**

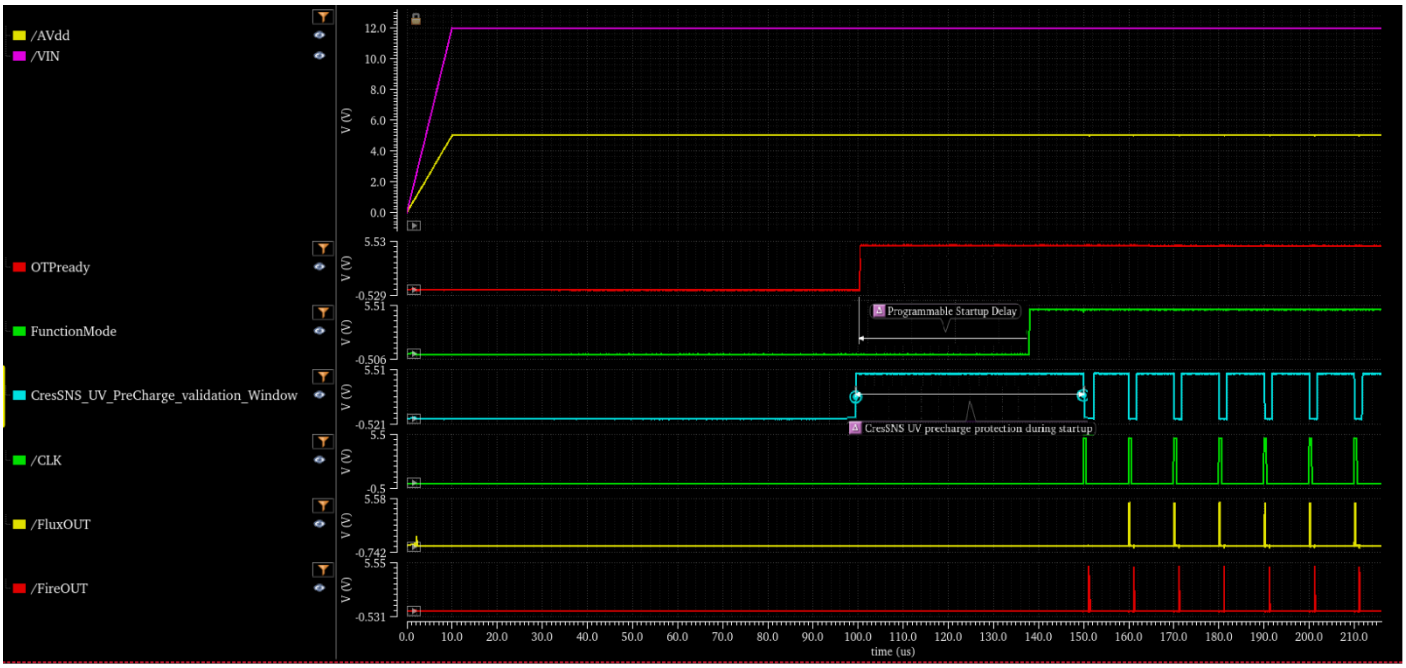


Figure 15: Startup Waveforms for OTPready, FunctionMode and the CresSNS Valid

Vin UV and OV Faults

Table 6 below shows the Fault Threshold Options for V_{IN} Undervoltage and *Table 7* shows the V_{IN} Overvoltage Fault options. If the V_{IN} UV fault is disabled, the SL2001 will continue to operate even with V_{IN} at zero. The undervoltage Faults are still Monitored to give an indication of V_{IN} falling below the intended supply voltage range. The SL2001 V_{IN} pin is rated for operation up to 24V; however, lower overvoltage threshold options are available.

V_{in} UV Voltage Options	Register 0x13	
	Bit 1	Bit 0
2.5V	0	0
4V	0	1
9.1V	1	0
11V	1	1

Table 6: V_{IN} UV Options

V_{in} OV Voltage Options	Register 0x13		
	Bit 5	Bit 4	Bit 3
30V	0	0	0
27V	0	0	1
17.5V	0	1	0
15.5V	0	1	1
13.5V	1	0	0
7.5V	1	0	1
6.5V	1	1	0
5.5V	1	1	1

Table 7: V_{IN} OV options

Cres Related Faults

The **Cres_SNS** pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in *Figure 18*. External resistor values of 6.2MΩ and 6.8MΩ have been characterized with the fault threshold voltages varying per *Table 9*. If you prefer to use a different value for the external resistor, a formula, *Equation 1*, is included in the Detailed Pin Descriptions section that is valid for external resistor values between 5MΩ and 8MΩ.

Please ensure that the external resistor can support the maximum voltage that will be seen on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action that the SL2001 takes when a fault as detected is described in *Table 8*.

Fault Condition	Action
V_{DD} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault Bit (Register 0x90 bit 0)
Cres Low After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit1)
Cres High After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit2)
Cres High Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit3)
Cres Low Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit4)
V_{IN} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit5)
V_{IN} High	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit6)
Over Temperature	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit7)

Table 8: Cres and V_{IN} Fault Reactions

Table 5: Programmable delays for OTP read mode to full Function mode.

Function	Cres Post Charge UV		Cres Post Charge OV		Cres Pre Charge UV		Cres Pre Charge OV	
Register	0x14, bits 4:2		0x16, bits 4:3		0x14, bits 1:0		0x14, bits 6:5	
Rsns value	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ
code 0	5.5V	6V	63V	69V	Vin-0.55V	Vin-0.12V	19V	21V
code1	7.5V	8.25V	105V	115V	Vin – 1.35V	Vin – 1V	37V	41V
code2	8.5V	9.5V	152V	167V	Vin – 1.65V	Vin – 1.3V	55V	61V
code3	9.5V	10.5V	185V	203V	Vin – 2.5V	Vin – 2.2V	75V	82V
code4	11.5V	12.5V						
code5	12.5V	14V						
code6	17V	18.5V						
code7	21.5V	23.5V						

Table 9: SL2001 Fault Trigger Level Settings for Cres Voltage

Figure 16 below, showing the Cres fault detection windows of one operation cycle under timing mode 1.
To ensure the Cres sense circuits do not false trip due to the noise of transient event, 450ns of blanking time is included after **FluxOut** goes low (for Cres post charge OV and UV fault checking). The valid Cres post charge OV and UV window will be 450ns after the **FluxOut** goes low and before the Charge time ends (the high time of the light blue waveform). It is important to set the Charge time to be longer than the blanking time with some margin. Otherwise, the detection will never be activated.

Similarly, for Cres pre charge OV and UV fault, the valid detection window will be 450ns after the **FireOUT** goes low and before an internal 10us timer expires (the high time of the dark blue waveform). The 10µs timer is included so that a normal amount of leakage on the VCAP voltage for a long amount of time (much greater than 10µs) will not incorrectly flag as a Cres pre charge UV fault.

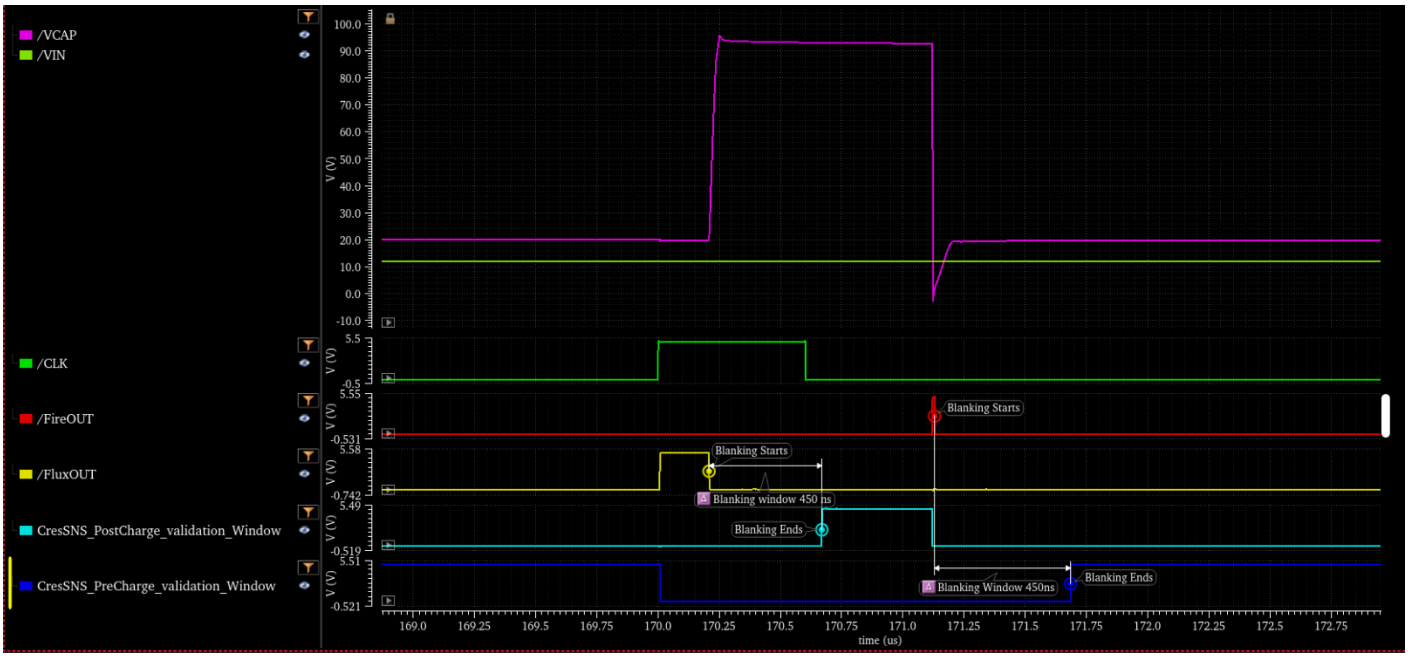


Figure 16: Fluxing and Firing Timing

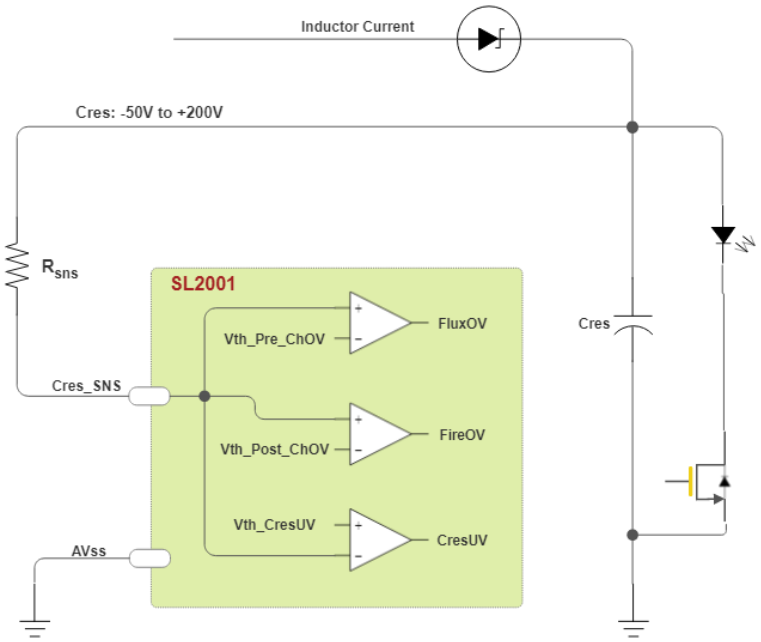


Figure 17: SL2001 Fault Diagram

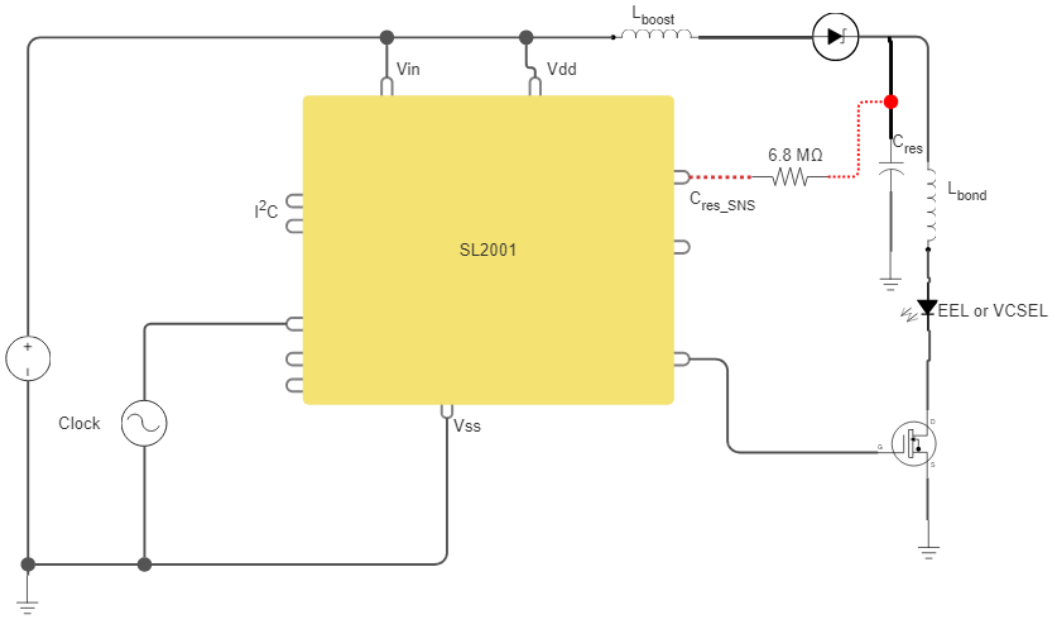


Figure 18: Cres Sense from the Anode Side

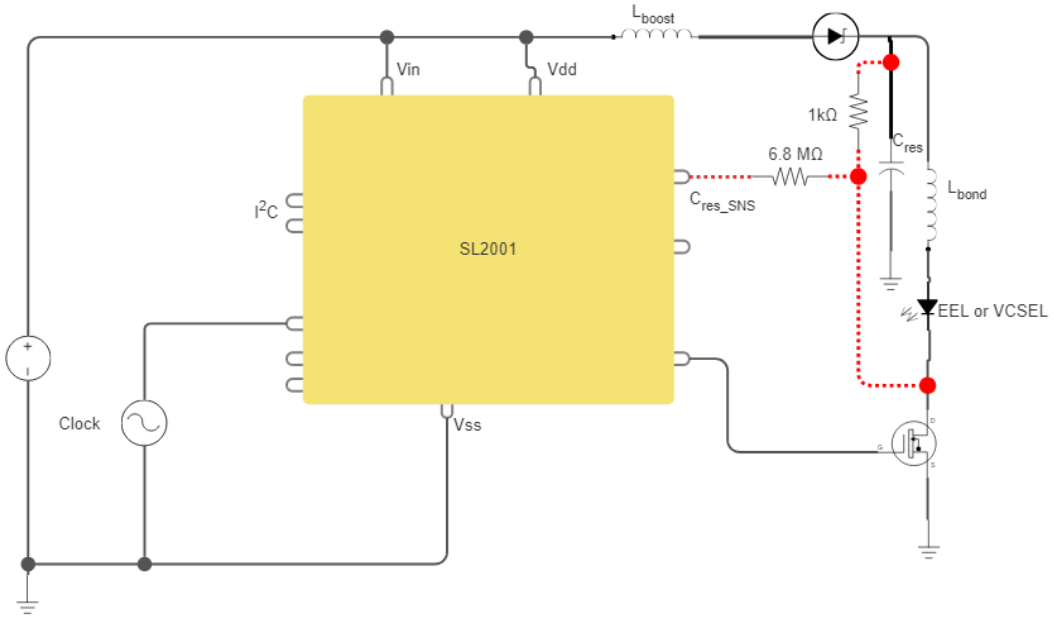


Figure 19: Cres Sense from the Cathode

It is also possible to sense at the Laser cathode as per *Figure 19*. In an application where short detection of Laser Firing GaN FET is critical, using a cathode sensing scheme will ensure a more accurate short circuit detection. For example, in *Figure 18*, when a weak short circuit occurs across the Laser firing GaN FET, it might only produce 100mA of current going through the Schottky diode. Therefore, the voltage drop across the Schottky diode isn't significant enough to be detected as a Cres UV pre-charge fault. This can cause the Laser diode to continue to emit light without being properly controlled. The Laser cathode sensing scheme ensures more accurate short circuit detection because of the additional voltage drop across the laser diode. It is recommended to add a resistor across the laser diode, as

shown in *Figure 19*. This enables the Laser cathode to settle faster and sync with the anode after the laser firing event. *Figure 20****Error! Reference source not found.*** shows an example waveform without any resistor between Laser Anode and Cathode. In this case the Cathode voltage doesn't reflect the true Anode (V_{CAP} node) voltage before or after Laser fired. The resistor value should be chosen based on the value of parasitic capacitance in the Laser firing path (including Laser Firing GaN C_{ds} and PCB parasitics), so that 3*RC time constant value is <300ns (after 3*RC time constants, the resistor has reached 95% of its final value). This ensures that the **CresSNS** input signal settles before the internal blanking time (for noise filtering) expires. *Figure 20* and *Figure 22****Error! Reference source not found.*** show the settling times for 1KΩ and 180Ω resistor values using the SLE2001-E01 evaluation board (modified for cathode sensing). For that board, the 1kΩ resistor provides a 3*RC time constant of ~1.26µs while the 180Ω resistor provides a 3*RC time constant of ~240ns. For that board, we recommend a resistor value that is less than or equal to 225Ω.

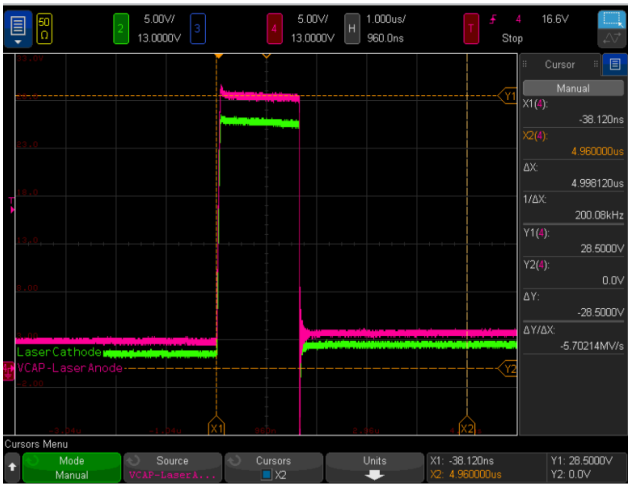


Figure 20: Laser Anode vs. Cathode without any resistor across Laser during operation

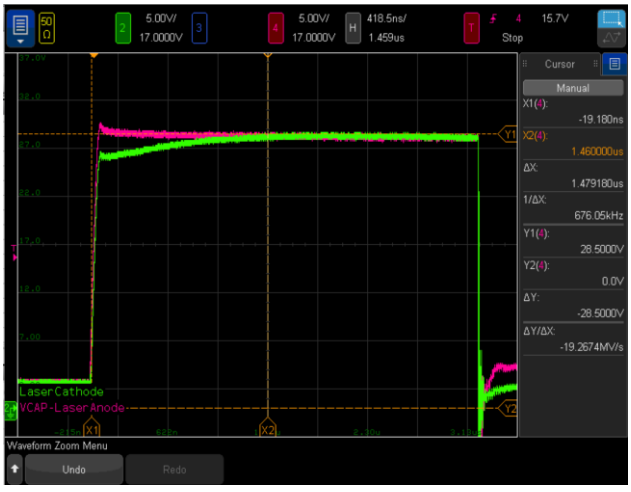


Figure 21: Laser Anode vs. Cathode with 1K ohm RES across Laser during operation

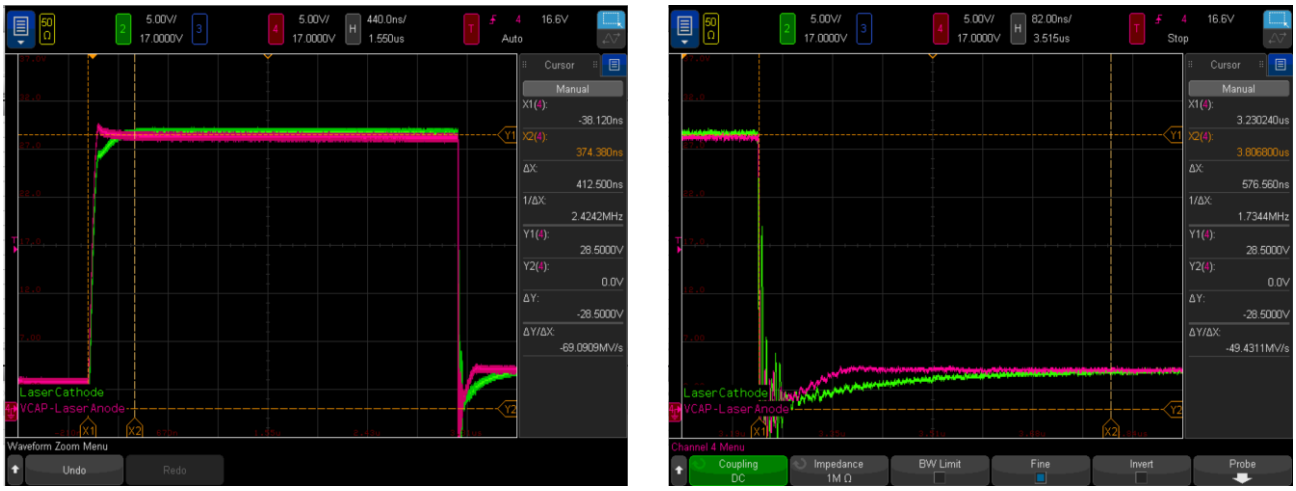


Figure 22: Laser Anode vs. Cathode with 180 ohm RES across Laser during operation

During the IC startup sequence, if V_{DD} and V_{IN} are biased separately and V_{DD} reaches 4.5V before V_{IN}, the SL2001 will be able to capture the short circuit between Laser firing GaN FET source and drain. The reaction to this fault condition, IC can be programmed to force the SL2001 to turn on the Fluxing GaN FET which directs current from V_{IN} to ground instead of going through the laser preventing the laser from emitting light until the SL2001 goes through a power cycle or is digitally reset via I²C. *Figure 23* gives an example waveform using this cathode sensing scheme. In this example, the system starts up and encounters a short circuit between the Laser cathode and ground (source and drain of the Laser firing GaN FET). This protection scheme is only available when V_{IN} is above 4.5V to ensure accuracy and prevent false tripping. When the V_{IN} supply is ramping up, Laser diode will start to conduct current via the short circuit. Once the V_{IN} is above 4.5V, the short circuit is detected, and protection is activated. In order to ensure the laser will stop emitting light, Register 0x05 bit 7 can be set to a 1 in order to latch the **FluxOUT** pin output to a high state and steer the V_{IN} current away from the laser to the ground path.

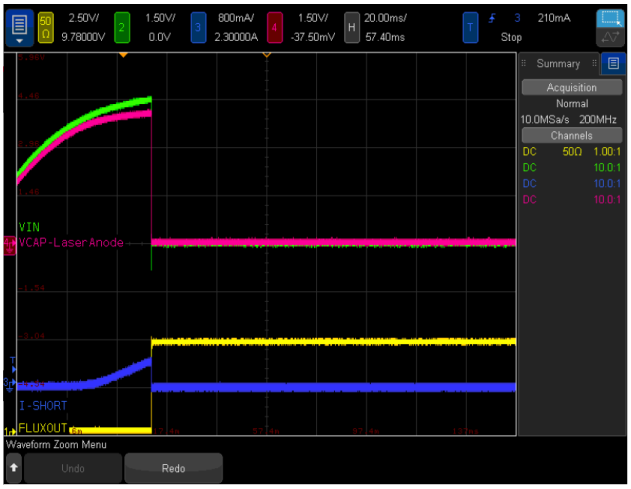


Figure 23: Laser firing GaNFET Short protection engaged after V_{DD} bias in place and during V_{IN} ramping up (cathode sense)

In applications where V_{DD} and V_{IN} supplies are combined the short circuit protection can still be triggered as shown in *Figure 24*. However, because V_{DD} and V_{IN} are sharing the same supply, if the Fluxing GaN is programmed to latch on due to a Cres UV fault, it may deplete V_{DD} and cause IC to go into power on reset and turn off the Flux GaN FET. If V_{IN}

and V_{DD} try to rise again, a repeat of these events will occur if the short is still present. An input power fuse is recommended in this case.

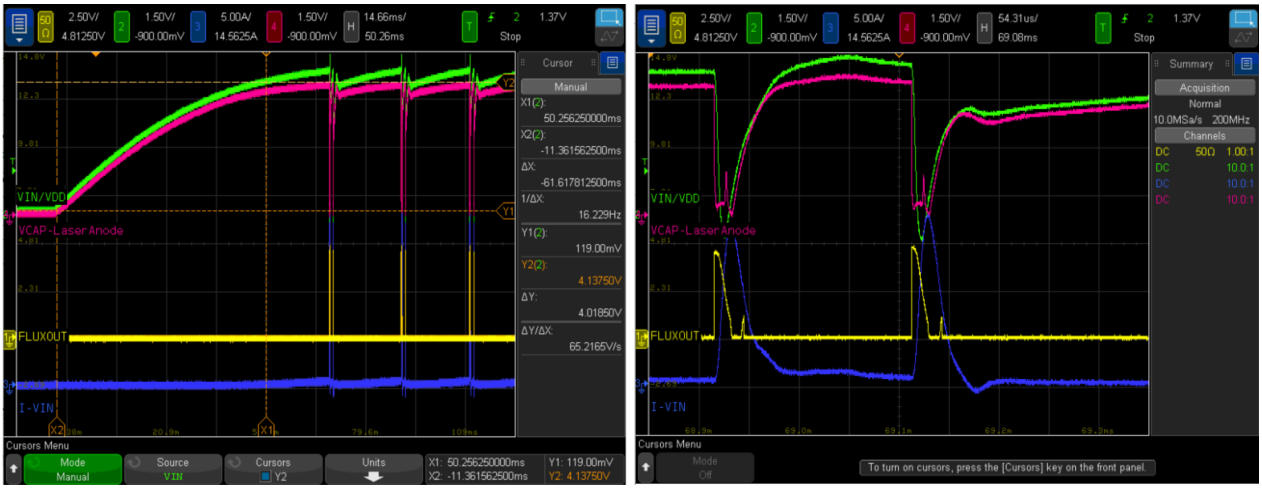


Figure 24: Laser firing GaNFET Short Circuit Protection engaged when VIN &VDD are biased from the same supply and zoom in view (cathode sense)

During normal operation, a short circuit between the Laser cathode and ground can also be detected by the IC. An example of this occurrence is depicted in *Figure 25* The short circuit for the waveforms of both figures occurs with a 1KHz repetition rate and is sensed using the laser cathode sensing scheme.

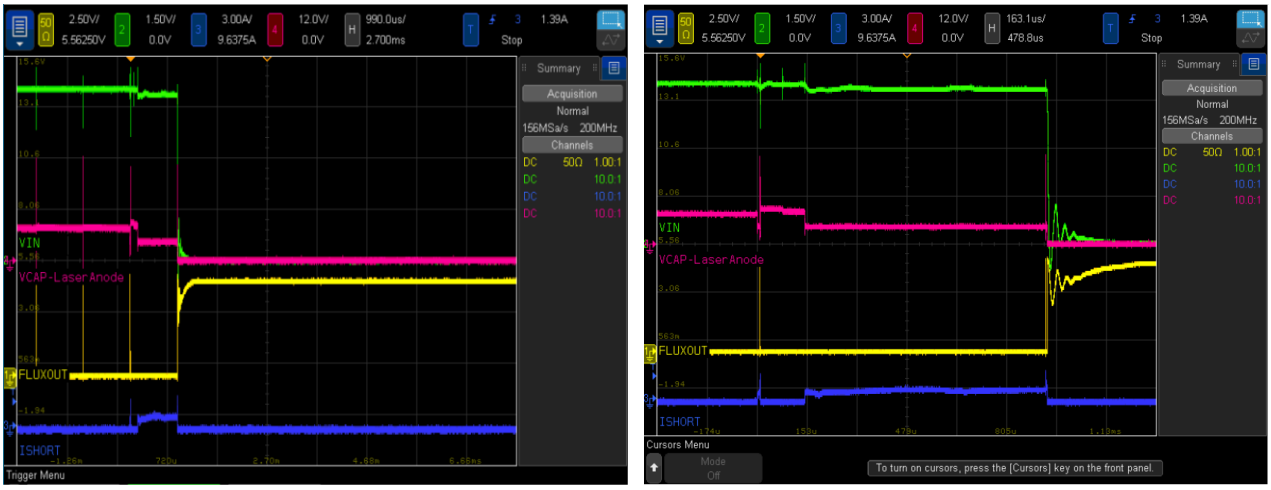


Figure 25: Laser firing GaNFET Short Circuit Protection engaged during operation when V_{IN} &V_{DD} are biased separately and zoom in view

Startup Fault Condition Examples

Condition 1:
AV_{dd} slew rate < 2V/100us, *SupplyOK Fault = True*

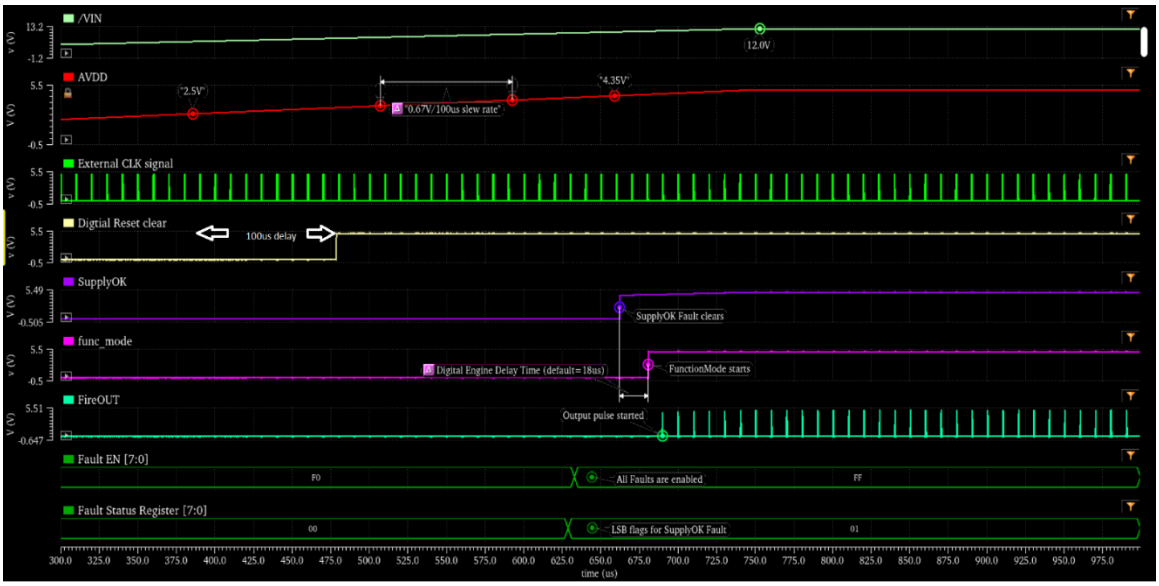


Figure 26: AV_{dd} slew rate is slower than 2V/100us

When **AV_{dd}** slew rate is slower than 2V/100us, the start-up completes with SupplyOK Fault asserted.
The Startup sequence completion is gated by a SupplyOk Fault. As **AV_{dd}** rises above the Supply Fault clear threshold, 18us (the programable delay time) after, normal operation starts.

Condition 2:
AV_{dd} slew rate > 2V/100us
SupplyOK Fault = False

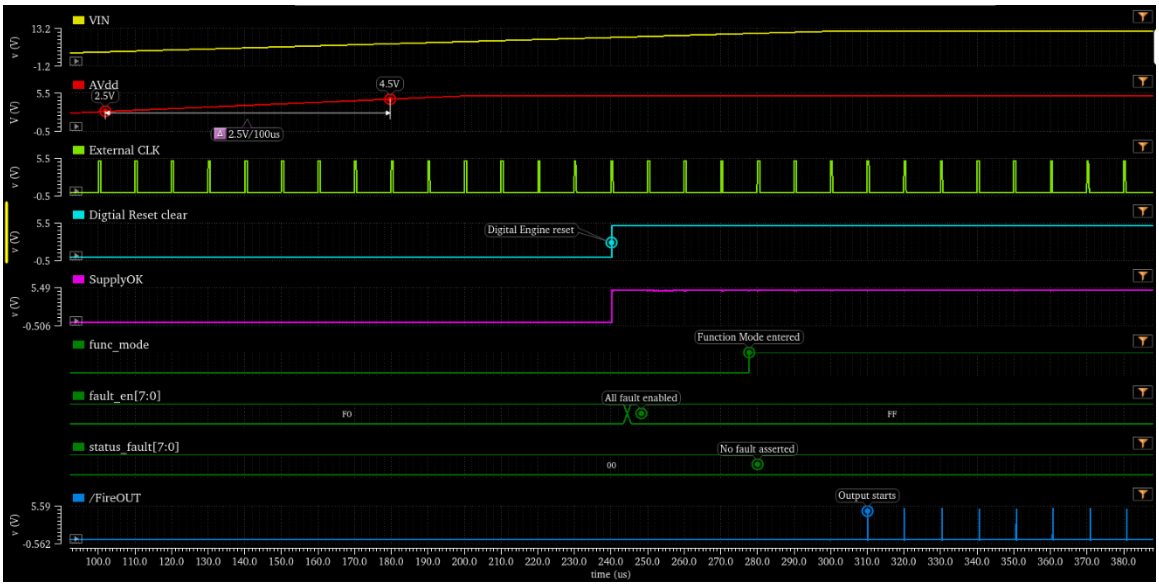


Figure 27: AV_{dd} slew rate is higher than 2V/100us

When the **AV_{dd}** slew rate is higher than 2V/100us, the start-up completes without a SupplyOK Fault being asserted. Normal operation starts after the startup sequence completes plus 18us of delay time.

Condition 3:

AV_{dd} = 5V before **V_{IN}** starts ramping: **V_{IN}** UV Fault = True, Startup Mode = Hiccup.

The **AV_{dd}** supply ramps up first and reaches 5V before the **V_{IN}** supply starts. A **V_{IN}** UV fault is reported and Hiccup Mode starts. After **V_{IN}** reaches the Vin UV clear threshold, the IC enters normal function Mode. The delay will be 28ms (Hiccup Delay Time).

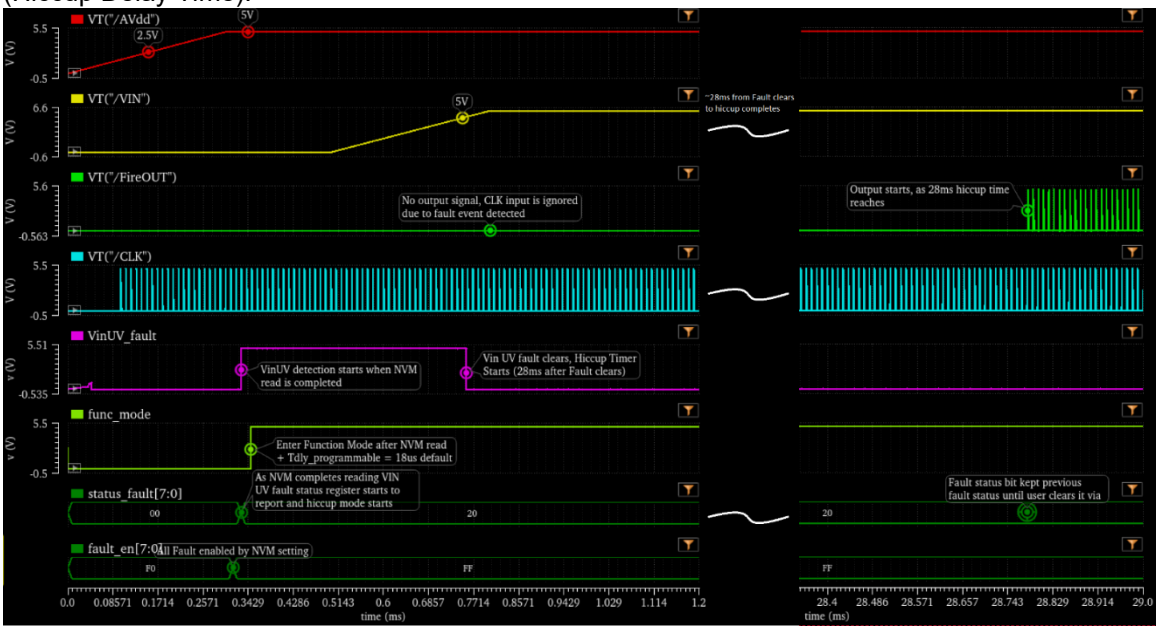


*Figure 28: **AV_{dd}** = 5V before **V_{IN}** starts ramping*

Condition 4:
AV_{dd} = V_{IN} = 5V;
V_{IN} UV thresholds set < 5V
Fault Status = None

AV_{dd} and **V_{IN}** are connected to one supply (Vin UV threshold is pre-programmed to lower than 5V for the rising edge). No Fault is reported during startup. The Output starts as soon as the device normal functioning starts.

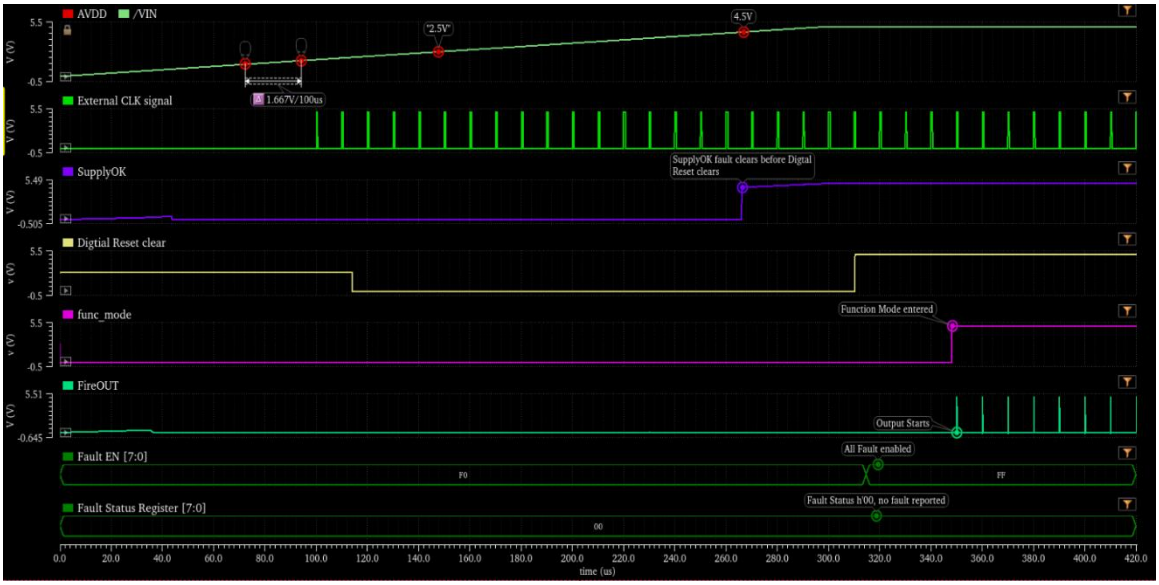


*Figure 29: **AV_{dd}** and **V_{IN}** are connected to one supply*

Condition 5:
VIN slew rate = 2V/100us
AVdd slew rate = 1.667V/100us
Fault Status = None
AV_{dd} and V_{IN} ramp together while the V_{IN} slew rate is 2V/100us and the AV_{dd} Slew Rate > 1.43V/100µs (see ***Error! Reference source not found.***). This will avoid tripping the V_{IN} $UV_{thresholdRising}$ = 5V when entering Functional mode.

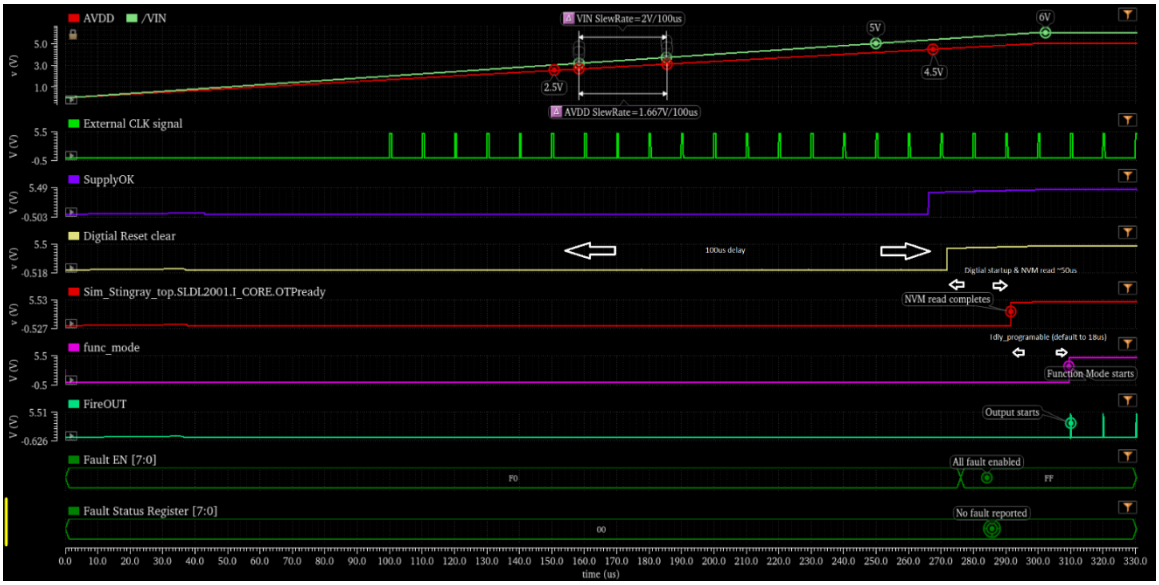


Figure 30: AV_{dd} and V_{IN} ramp together

Reference Design

A example reference design of an evaluation board using SL2001 is shown below. Evaluation boards are available using both a 400W EEL laser (SLE2001-E01) and a 800W VCSEL laser (SLE2001-V01).

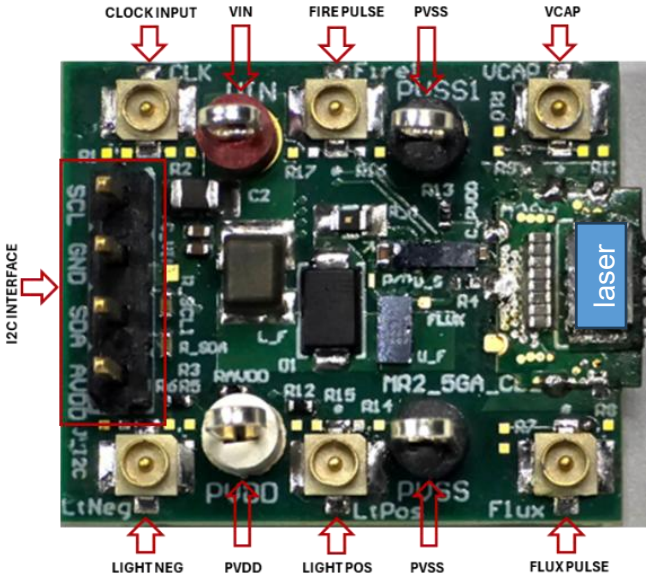
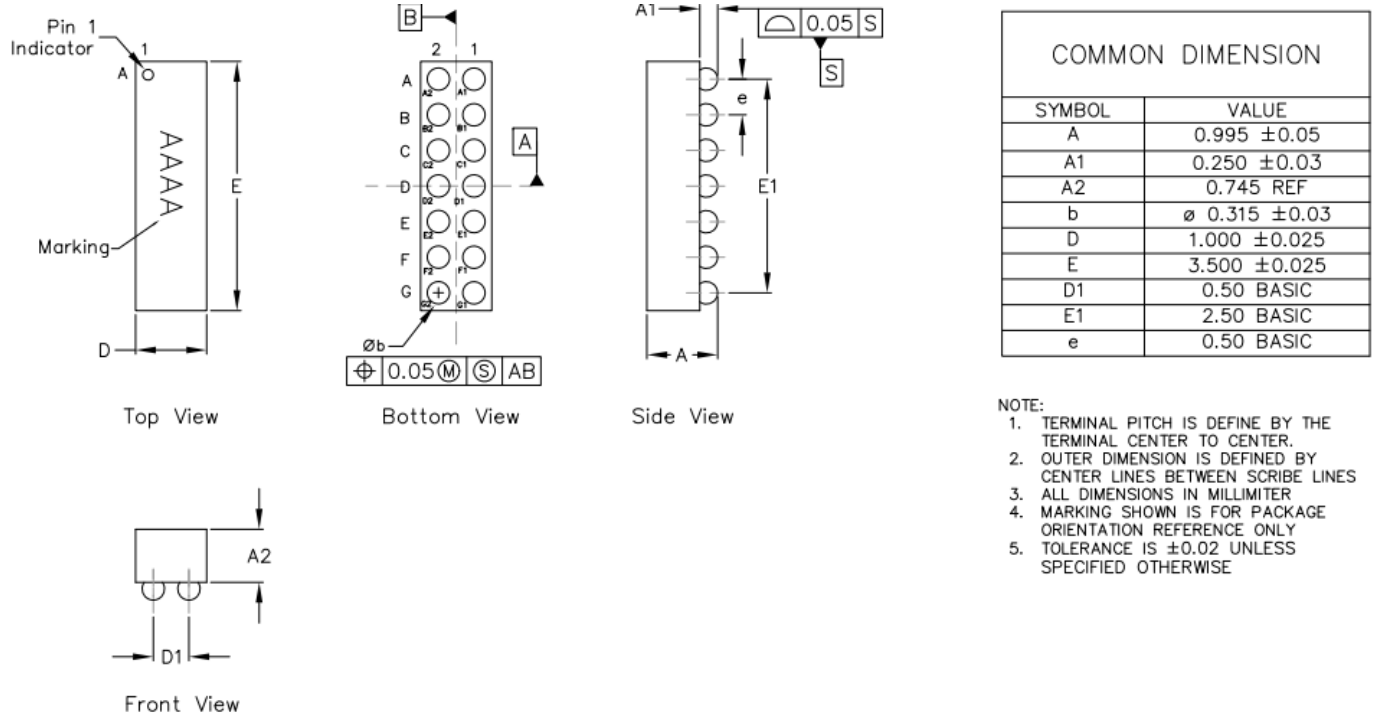


Figure 31: SL2001 Evaluation Board

SL2001A Final Datasheet

Package Dimensions



COMMON DIMENSION	
SYMBOL	VALUE
A	0.995 ±0.05
A1	0.250 ±0.03
A2	0.745 REF
b	ø 0.315 ±0.03
D	1.000 ±0.025
E	3.500 ±0.025
D1	0.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC

NOTE:
1. TERMINAL PITCH IS DEFINE BY THE TERMINAL CENTER TO CENTER.
2. OUTER DIMENSION IS DEFINED BY CENTER LINES BETWEEN SCRIBE LINES
3. ALL DIMENSIONS IN MILLIMITER
4. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY
5. TOLERANCE IS ±0.02 UNLESS SPECIFIED OTHERWISE

Figure 32: Package Dimensions

Product Ordering Information

Part Number	Package	Feature	Shipping Method
SL2001A-WHS	14 Pin bumped flip chip	1kW Peak Power Laser Driving System with Integrated Timing Controller, Boost Voltage Generator and Fault Protection for Laser Time-of-Flight Measurement Systems	2,500 pcs Tape & Reel

SL2001A Final Datasheet

Revision History

Revision	Date	Author	Note
1.0	12/10/2025	AZ	GPR Release