SL2002A Final Datasheet

Features

- Flexible architecture can provide laser FWHM pulses less than 2ns
- Dual Drive Outputs Support Peak Power up to 200W
- High charging efficiency from a 2.8V to 5.5V supply
- Integrates needed blocks for Charging and Firing Resonant-Mode Diode Lasers utilizing either EEL Diodes or VCSEL Arrays
- Integrated GaN/MOS Drive for Charging a Resonant Capacitor
- Inductor Current Control offers precise Resonant Capacitor Energy even with Input Voltage Fluctuations
- < 5 mW System No Load Power Consumption
- Up to 10 MHz Rep Rate limited by temperature rise in laser and other board components
- Dual Polarity LIGHT Output signal to indicate when laser fires with extremely low jitter (time error jitter < 0.1ns)
- Minimal external components enable extremely integrated and efficient layout
- Integrated I^2C interface for Output Power Control and Fault monitoring
- 7 MTP Bytes (3 time programmable) for fault and timing settings
- 219 OTP Bytes for customer usage
- 1 mm x 3.5 mm WLCSP Package

Product Description

The SL2002 is an Integrated Timing Controller, Boost Voltage Generator, and Driver for Laser Time-of-Flight Measurement Systems employing Edge Emitting Laser Diodes or VCSEL Diodes.

This device provides the ease-of-design of a simple resonant flash TOF laser system but is integrated together with a boost charger and proprietary charge control to efficiently charge the resonant capacitor to the optimum voltage from a 2.8V – 5.5V supply..

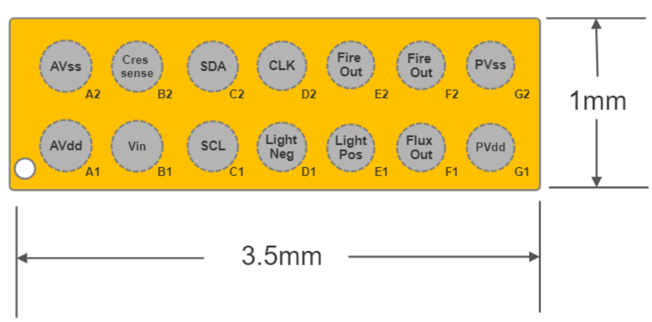
The integrated Pulse Timing Controller uses a proprietary Architecture to provide Laser Diode pulses less than 3 ns wide and capable of providing 200 watts of Peak Light power. An External MOSFET or small GANFET provides the “Flash” signal to fire the laser. Integrated drivers provide the necessary signal for driving GANFETs or MOSFETs.

The Resonant Capacitor is charged during each pulse cycle via an internal boost charger. This integrated charging architecture minimizes losses normally associated with transferring charge from standard High Voltage Supply Rails. The supply voltage for the charger can be as low as 2.8 volts and still achieve laser diode voltages of > 100 volts. No external Boost Regulator is required.

Multiple Time Programmable NVM and run time programmable I^2C registers allow the flexibility to achieve the highest laser light power with optimum efficiency over a large range of applications. Optional automatic variation of resonant capacitor charge time can maintain a constant laser output power over a 2.8V to 5.5V input voltage level.

Applications

- Laser TOF Measurement Systems
- Range Finding
- 3D Mapping
- Industrial Sensors



Pin Out

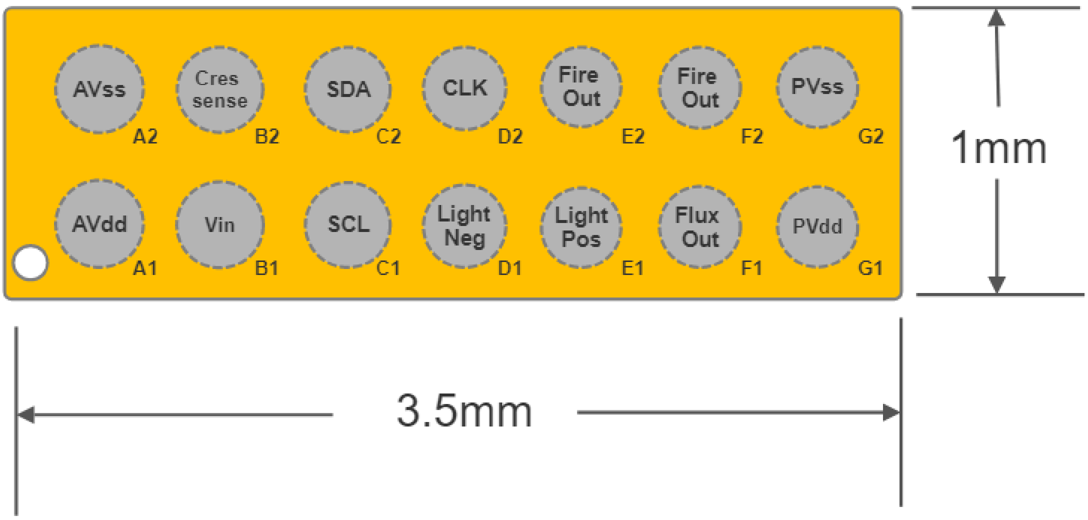


Figure 1: SL2002, 14 ball WCSP (0.5mm ball pitch) – Device Top View (bumps down)

Pin Definitions

Pin #	Name	Voltage Category (Vdc)	Description
A1	AV_{DD}	LV: (5V)	Analog supply for inputs
A2	AV_{ss}	LV (0)	analog ground for inputs
B1	V_{IN}	MV (8.5V)	inductor input voltage sense point
B2	C_{res} _SNS	LV (5V)	Cres voltage sense via external impedance
C1	SCL	LV (5V)	I^2C clock pin
C2	SDA	Output LV	I^2C data pin
D1	LightNeg	Output LV	Output indicating Laser Firing. low on rising edge of FireOUT and stays low for 75ns or until FireOUT goes low
D2	CLK	LV (5V)	Dual function timing input for capacitor charge and laser firing (see *Figure 3* and *Figure 4*)
E1	LightPos	Output LV	Output indicating Laser Firing. high on rising edge of FireOUT and stays high for 75ns or until FireOUT goes low
E2	FireOUT	Output LV	Output Drive for MOSFET or EGaN FET for External Cathode Clamp
F1	FluxOUT	Output LV	Output Drive for MOSFET or EGaN FET for inductive charging switch
F2	FireOUT	Output LV	2^{nd} FireOUT pin (shorted to pin E2) for lower board impedance to FET gate
G1	PV_{DD}	LV: (5V)	Power Supply for gate drive outputs
G2	PV_{ss}	LV (0)	Power Resonant Supply Voltage Rail Return for gate drive outputs

Table 1:SL2002 Pin Definitions

Functional Block Diagram

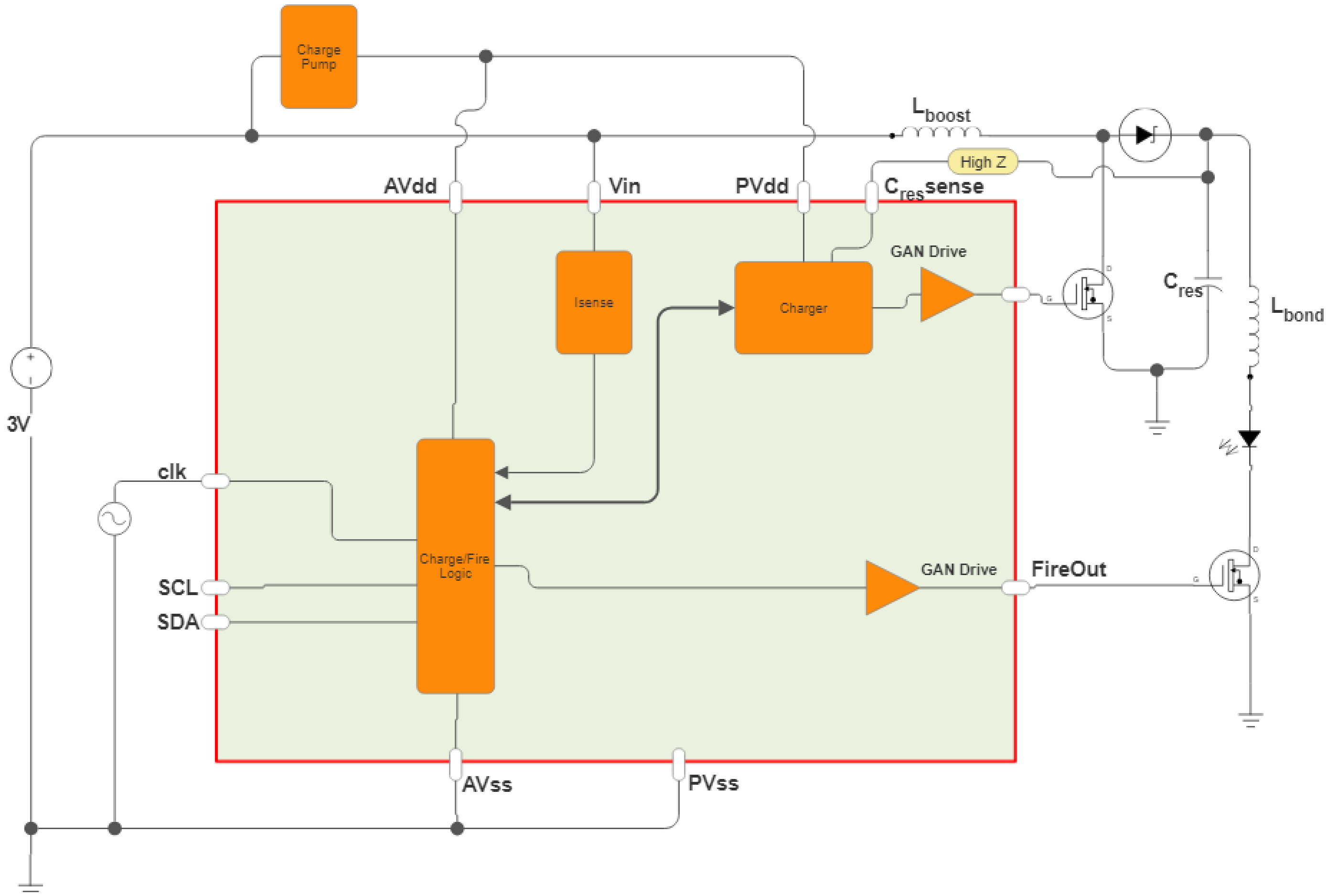


Figure 2: Functional Block Diagram

Absolute Maximum Ratings Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Max.	Units
Pin Voltages - Inputs	CLK		-0.3	AV_{DD}+0.3	V °C
	AV_{DD}		-0.3	6.5	
	AV_{ss}		-0.3	0.3	
	PV_{DD}		-0.3	6.5	
	PV_{ss}		-0.3	0.3	
	SCL, SDA		-0.3	AV_{DD}+0.3	
	C_{res} _SNS		-0.3	AV_{DD}+0.3	
	V_{IN}		-0.3	8.5(3)	
Pin Voltages - Outputs Storage Temperature	FireOUT		-0.3	6.5	
	FluxOut		-0.3	6.5	
	T_{STG}		-50	150	
Junction Temperature	T_J		-40	150	°C V
Lead Temperature	T_{LEAD}			260	
Electrostatic Discharge (ESD) Protection (3)	V_{ESD}	HBM, Human Body Model per ANSI/ESDA/JEDEC JS-001	-2000	2000	
Electrostatic Discharge (ESD) Protection (2) Parameter	V_{ESD} Symbol	Charged-device model (CDM), per JEDEC specification	-500	500	V

Notes:

1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
3) Needed to accommodate NVM programming

Thermal Information [Note 1]

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient	$R_{\Theta JA}$	30	°C/W
Thermal Resistance Junction to Board	$R_{\Theta JB}$	12	

Notes:

1) Simulated on 2S2P JEDEC 51-7 board.

Recommended Operating Conditions [Note 1]

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{DD} Supply Input Voltage	V_{VDD}		4.5	5	6.0	V
V_{IN} Voltage	V_{IN}		2.8		5.5	V
AV_{DD} Bypass Capacitor	C_{AVDD}		-	0.1	-	µF
PV_{DD} Bypass Capacitor	C_{PVDD}		-	10	-	µF
V_{IN} Bypass Capacitor	C_{VIN}		-	22	-	µF
Operating Junction Temperature	T_J		-40		125	°C

Notes:

1) Device electrical characteristics are not guaranteed outside the recommended operating conditions.
2) Note that many electrical characteristics are specified for 4.5V < V_{DD} < 5.5V

Electrical Characteristics

(Unless otherwise specified, 4.5V < AV_{DD} < 5.5V, AV_{DD} = PV_{DD}, TJ = -40 °C to 125 °C recommended operating conditions.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Current (VDD)						
Input Supply Current, No Load	$I_{VDDNL)}$	Laser fire freq < 1kHz, DAC codes 150	-	1.0	-	mA
Input Supply Current, Pulsing	$I_{VDD(SW)}$	Laser fire freq = 250kHz?, Fire Out cap = 100pF[1]	-	3	-	mA
FireOut Drive Output – the two FireOut bumps are shorted on die						
FireOut Resistance Pull Down	$V_{OL\_FireOut}$	$I_{OL\_FireOut}$ = 100mA			180	mΩ
FireOut Resistance Pull Up	$V_{OH\_FireOut}$	$I_{OH\_FireOut}$ = 100mA			250	mΩ
Peak Sink Current	$I_{OL\_FireOut}$	$V_{OL\_FireOut}$ = 5V[1]		12	-	A
Peak Source Current	$I_{OH\_FireOut}$	$V_{OH\_FireOut}$ = 0V[1]		10		A
FluxOut Output						
FluxOut Resistance Pull Down	$V_{OL\_FluxOut}$	$I_{OL\_FluxOut}$ = 100mA			720	mΩ
FluxOut Resistance Pull Up	$V_{OH\_FluxOut}$	$I_{OH\_FluxOut}$ = 100mA			1	Ω
Peak Sink Current	$I_{OL\_FluxOut}$	$V_{OL\_FluxOut}$ = 5V[1]		3	-	A
Peak Source Current	$I_{OH\_FluxOut}$	$V_{OH\_FluxOut}$ = 0V[1]		2.5		A
LIGHT Drive Output – same parameters for LightPOS & LightNEG pins						
LIGHT Resistance Pull Down	R_{DSL_LIGHT}	I_{OL_LIGHT} = 100mA			2.88	Ω
LIGHT Resistance Pull Up	R_{DSH_LIGHT}	I_{OH_LIGHT} = 100mA			4	Ω
Peak Sink Current	I_{OL_LIGHT}	V_{OL_LIGHT} = 5V[1]		1.5	-	A
Peak Source Current	I_{OH_LIGHT}	V_{OH_LIGHT} = 0V[1]		1.25		A

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FireOut Switching Parameters						
Maximum Switching Frequency (1)	f_{SW_MAX}	Note 1			10	MHz
Minimum On Time	TON_{MAX}	Minimum on time of the FireOut FET gate driver[1]	1			ns
LightPos & LightNeg output parameters						
Delay from FireOut rise to LightPos rise or LightNeg Fall		crossing threshold through 50% of Vdd[1]	-1		1	ns
FireOut to LIGHT rise cycle to cycle jitter		crossing threshold through 50% of Vdd with 100pF load on FireOUT & 10pF load on LightPos/Neg[1,2]	-100		100	ps
LightPos high & LightNeg low pulse width		crossing threshold (AV_{dd} – Avss) / 2	35		105	ns
Input Signal Parameters						
C_{res}SNS resistance to AV_{ss}		While operating; forced to 0.2V		22		kΩ
CLK input rising threshold			1.7		2.6	V
CLK input falling threshold			1.1		1.8	V
CLK input voltage hysteresis			0.5		1	V
SDA/SCL input rising threshold					1.7	V
SDA/SCL input falling threshold			0.45			V
I^2C SCL Frequency					1	MHz
Timing Parameters						
CLK high to FluxOUT		CLK >50% to FluxOUT > 50%		5		ns
FluxOUT PW range from FluxOUT>50% to FluxOUT<50%		typ values for range, see Basic Timing Description Section explanation [1]	5		2800	ns
FluxOUT PW Accuracy from FluxOUT>50% to FluxOUT<50%		DAC code h’A8 on Flux Time Reg 100pF on FluxOUT, V_{IN}=5V	188	200	212	ns
FluxOUT PW jitter from FluxOUT>50% to FluxOUT<50%		DAC code h’A8 on Flux Time Reg 100pF on FluxOUT, V_{IN} =5V[1,2]	-1		+1	%
CLK high to FluxOUT jitter from Clock>50% to FluxOUT>50%		DAC code h’A8 on Flux Time Reg cycle to cycle jitter; 100pF on FluxOUT[1,2]	-2.5		+2.5	ns
FluxOUT rise time		20% to 80% of PV_{DD} 100pF on FluxOUT[1,2]		0.45		ns
FluxOUT fall time		80% to 20% of PV_{DD} 100pF on FluxOUT[1,2]		0.45		ns
FluxOut Low to FireOut High range from FluxOUT<50% to FireOUT>50%		typ values for range, see Basic Timing Description Section explanation [1]	10		2800	ns
FluxOut Low to FireOut High Accuracy from FluxOUT<50% to FireOUT>50%		DAC code h’A7 on Charge Time Reg 100pF on FluxOUT & FireOUT[3]		200		ns
CLK low to FireOut		CLK <50% to FireOUT > 50%[1]		20		ns
FireOut PW range from FireOUT>50% to FireOUT<50%		typ values for range, see Basic Timing Description Section explanation [1]	1		320	ns
FireOut PW Accuracy from FireOUT>50% to FireOUT<50%		DAC code h’80 on Fire Time Reg, 100pF on FireOUT, VDD=5V, T=25C[1]	4.25	5	5.75	ns
		same conditions as above -40C<Tj<125C[1]	4	5	6	ns
FireOut PW jitter from FireOUT>50% to FireOUT<50%		DAC code h’7C on Fire Time Reg 100pF on FireOUT[1,2]	-4		+4	%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CLK low to FireOut jitter from Clk<50% to FireOUT>50%		DAC code h'7C on Fire Time Reg cycle to cycle jitter; 100pF on FireOUT[1,2]	-5		+5	ns
Supply Voltage Threshold and Fault Protection Parameters						
AV_{DD} & PV_{DD} rising threshold			4.13	4.3	4.5	V
AV_{DD} & PV_{DD} falling threshold			3.9	4.05	4.2	V
AV_{DD} & PV_{DD} Vth Hysteresis				0.26		V
delay from V_{DD} rising threshold to laser firing enabled [3]					1	ms
V_{IN} Over Voltage accuracy		V_{IN} > 6.5V	6	6.5	7	V
V_{IN} Under Voltage accuracy		V_{IN} <2.5V	2.3	2.5	2.7	V
Thermal Shutdown (OTP)	T_{SD}	Note 1		150		°C
Thermal Shutdown Hysteresis	T_{HYS}	Note 1		20		°C
C_{res} pre–Charge OV		Rsense = 6.8MΩ	17.85	21	24.15	V
C_{res} post Charge OV		Rsense = 6.8MΩ	97.75	115	132.25	V
C_{res} pre-charge UV		Rsense = 6.8MΩ	V_{IN}-1.085	V_{IN}-1.3V	V_{IN}-1.515V	V
C_{res} post-charge UV		Rsense = 6.8MΩ, REG0x14 bits 4:3=00	4.5	6	7.5	V
C_{res} post-charge UV		Rsense = 6.8MΩ, REG0x14 bits 4:3=11	13.87	18.5	23.13	V

Notes:

1) Guaranteed by design and characterization, not production tested
2) cycle to cycle jitter is specified for no change in any environmental conditions. It shows a Gaussian distribution with 3 sigma numbers specified as limits
3) Only valid for operating mode where CLK falling edge does NOT trigger the laser to fire

Contents

Figures

Overview

The SL2002 is a fully integrated Resonant Mode Controller for Driving EEL or VCSEL Laser Diodes. It uses a current source to provide a predetermined amount of charge to the laser resonant capacitor each cycle from a low input voltage source allowing the resonant capacitor voltage to increase as a function of the amount of charge. It is possible to achieve high resonant capacitor voltage from a relatively low input **V_{IN}**. The small Resonant Capacitor values which match the small predicted parasitic inductance values can be used without need for a high voltage input rail. This eliminates the need for a boost converter to provide the needed high Resonant Capacitor Voltage. A series inductor is used to provide the current to charge the Resonant Capacitor to the needed voltage for the Laser Diode resonant circuit. The stored energy in the Resonant Capacitor is then transferred to the Laser Diode during the "Firing" phase. The SL2002 monitors the input Voltage (**V_{IN}**) and adjusts the amount of time the input inductor is "fluxing" to compensate for variations in **V_{IN}**. Fault trigger levels can be set for **V_{IN}** undervoltage and overvoltage. The SL2002 also monitors the voltage on the Resonant Capacitor (**C_{res}**) for under and over voltage conditions. A description of the Fault detection and operation is shown in the section *Protection and Fault Information*. High current drive for either MOS or GaN FETs is also integrated as well as indicators for light pulse start. The device can also detect and shunt current away from the laser if the firing FET fails for Eye Safety.

Detailed Pin Descriptions

Pins A1: **AV_{DD}** and **A2**: **AV_{ss}**

AV_{ss} is the Main ground return for the analog circuitry and the Light output signals. This circuitry is supplied by **AV_{DD}**, a decoupling capacitor between **AV_{DD}** and **AV_{ss}** should be placed as close as possible to the IC. **AV_{ss}** should nominally be tied to board ground within a few millimeters of the SL2002 in a board location that is outside of the current path between the ground input to the board and the ground of the resonant capacitors. Special attention should be paid to preventing switching noise between **AV_{ss}** and the ground pins of the chip that is receiving the **LightPos** and **LightNeg** output signals.

Pins G1: PV_{DD} and G2: PV_{SS}

PV_{ss} is the main power ground return for the gate drive circuitry. The gate drive circuitry is supplied by **PV_{dd}**. A decoupling capacitor between **PV_{DD} and PV_{ss}** should be placed as close as possible to the IC. **PV_{ss}** should be tied to the power ground plane in a manner to minimize inductive voltage ringing between the GaN FET used for laser firing (1^{st} priority) as well as minimize the inductive voltage ringing between the GaN FET used for inductor current ramp (2^{nd} priority).

Pin B1: V_{IN}

This pin is used to sense the inductor input voltage for Fault recognition as well as to maintain a constant inductor peak current.

Pin B2: C_{res}SNS

The **C_{res}SNS** pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in *Figure 21* for sensing at the laser anode and in *Figure 22* for sensing of the laser cathode. Fault thresholds are outlined in the electrical characteristics section using a 6.8MΩ external resistor. External resistor values between 5MΩ and 8MΩ are valid and will change the Cres fault threshold values shown in the Electrical Characteristics section per the equation below.

Equation 1: $$Cres\ Fault\ Thresold = Fault\ Threshold\ with\ 6.8M\Omega * \frac{External\ Rcres\ value}{6.8M\Omega}$$

Please ensure that the external resistor can support the maximum voltage on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2002 takes when a fault is detected is described in *Table 5.*

Pins C1: SCL and C2: SDA

These are the Clock and Data pins for I^2C interface. The I^2C Interface is always accessible. High level register descriptions are shown in *Table 4*. Four selectable I^2C addresses are available for the SL2002. These are selected by changing bits 1 & 0 in register address 0x16, explained in *Table 2*. These bits can be changed during operation via an I²C command, in which case the address will change immediately such that all subsequent I²C communication until the part is powered down will use the new address. The address bits can also be loaded into the 3-time programmable MTP such that the I²C address option will always be loaded at part start-up.

Register 0x16 bit1 bit0	I²C Address
00	0001001x
01	0101001x
10	1001001x
11	1101001x

Table 2: I²C Startup Addresses

Pins D1: LightNeg and E1: LightPos

These pins provide an indication of the **FireOUT** signal going high with an extremely small amount of signal jitter from period to period (3 sigma jitter <100ps).

Pin D2: CLK

This multi-function pin supplies the main clock to the pulse timing generator. The rising and falling edges of the clock can be programmed to trigger the gate drive outputs in 2 different modes as described in the timing control section below in *Figure 3* and *Figure 4*.

Pins E2 and **F2**: **FireOUT**

These pins provide an extremely fast gate drive signal with adjustable pulse width between 0.5ns and 100ns for the GaN or MOS Gate Drive. Two adjacent pins are used to reduce the parasitic inductance on the die and on the board.

Pin F1: FluxOUT

This pin provides a fast gate drive signal with adjustable pulse width between 5ns and 1µs for the GaN FET that is used to ramp current in the inductor and charge the resonant capacitor.

Timing Description: Inductor Flux, Cres Charge and Laser Fire

Two Timing modes allow the option to trigger the charging of the resonant capacitor followed by the firing of the laser from a **CLK** rising edge (Mode 1 not dependent on **CLK** duty cycle) or to trigger the charging the resonant capacitor from the **CLK** rising edge and trigger the firing of the laser from the **CLK** falling edge (Mode 2).

Mode1 Timing Steps (Register 0x14 bit 7 = 0)

The **CLK** rising edge triggers **FluxOUT** to rise, starting the Flux time (inductor current ramp). The Flux time “Tflux(ns)” is controlled by register 0x10 with 2.5% steps from 5ns to 2.8µs. *Figure 8* shows the inversely proportional behavior of the Flux Time to the $\mathbf{V_{IN}}$ voltage. The orange curve has longer Flux time due to the lower $\mathbf{V_{IN}}$ voltage of 2.8V while the red curve has shorter Flux time due to the higher $\mathbf{V_{IN}}$ voltage of 6V.

The $\mathbf{C_{res}}$ Charge Time starts with the falling edge of the **FluxOUT** signal. The Charge time “Tcharge(ns)” is controlled by register 0x11 with 2.5% steps from 10ns to 2.8µs as shown in *Figure 12*. At the end of the Charge Time, the **FireOUT** signal goes high to begin the Fire time. The Fire time “Tfire(ns)” is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in *Figure 13*.

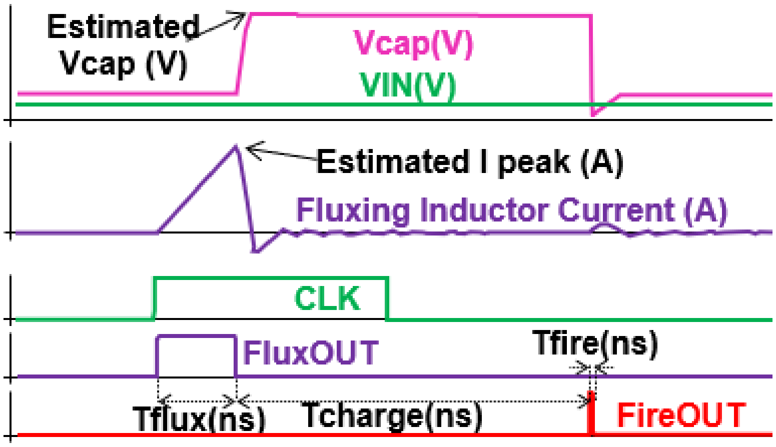


Figure 3: Mode1 Timing

Mode2 Timing Steps (Register 0x14 bit 7 = 1)

The **CLK** rising edge triggers the **FluxOUT** signal to rise, starting the Flux time (inductor current ramp).The Flux time "Tflux(ns)" is controlled by register 0x10 with 2.5% steps from 5ns to 2.8µs as shown *Figure 8*.The Charge Time "Tcharge(ns)" is controlled by the pulse width of the **CLK** input pin. At the falling edge of the CLK input pin, the **FireOUT** signal goes high to begin the Fire time. The Fire time "Tfire(ns)" is controlled by register 0x12 with 2.5% steps from 1ns to 320ns as shown in *Figure 13.*

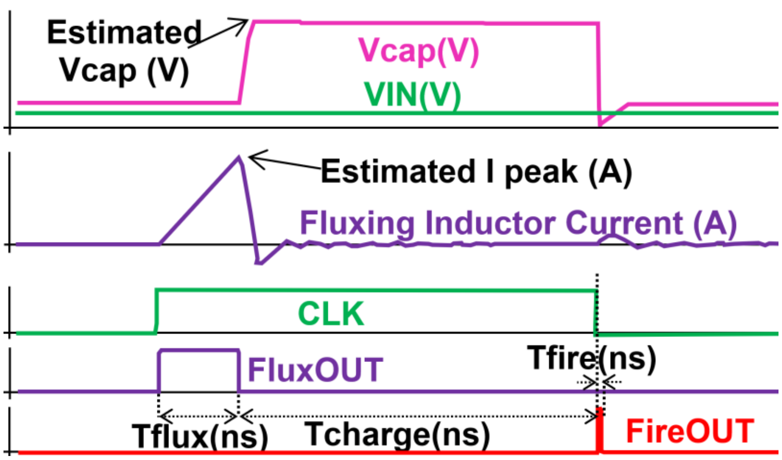


Figure 4: Mode2 Timing

The timing for Fluxing is controlled by the circuit in *Figure 5*. Identical circuits are used to set the timing for Charging (mode1 only) and Firing. A current I1 is set-up by forcing a voltage (Vref1) across a DAC programmable resistance value. That current I1 is then mirrored to a current I2 and used to charge a capacitance to a voltage level (Vref2). When the **CLK** signal goes high, the **FluxOut** signal will go high until the capacitor is charged to the Vref2 level. The **FluxOut** high time will follow *Equation 2*.

$$\text{Equation 2}: Fluxout\ high = \frac{C * Vref2 * Rdac}{Vref1 * Gmirror}$$

The **FluxOut** high time will change proportionally to a change in the DAC resistance value (Rdac). The **FluxOut** high time will change inversely proportional to a change in the voltage of Vref1 or the gain of the current mirror (Gmirror).

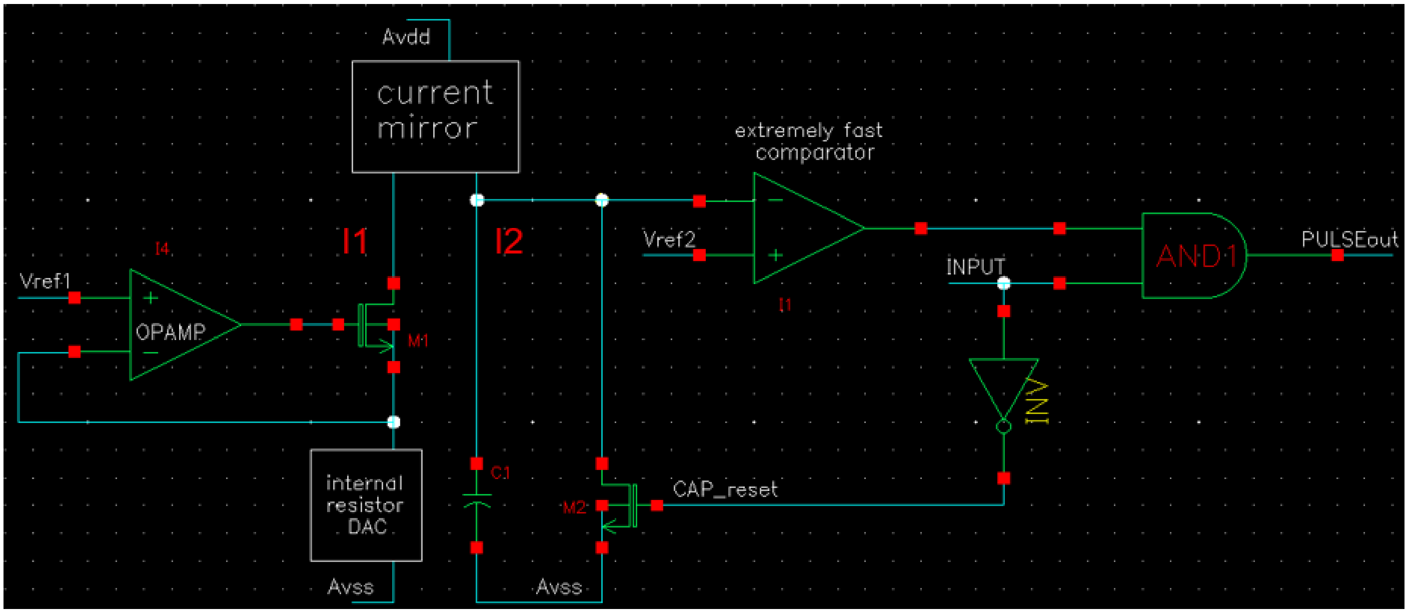


Figure 5: Flux Timing Generation

Three 8-bit registers (0x10h, 0x11h, 0x12h): FluxTime, ChargeTime and FireTime correspond to DACs for each of these timing parameters. Their resistor value increases by ~2.5% for each DAC step, with a minimum resistor value of 2kΩ and a maximum resistor value of 1.085MΩ with each resistor value set by *Equation 3* for Rdac codes from zero to 255.

Equation 3: $Rdac\ value = 2k * 1.025^{(Rdac\ code)}$

The Rdac value changes linearly on a log scale as shown in the graph in *Figure 6*. Note that the Rdac code is an exponent in the equation above.

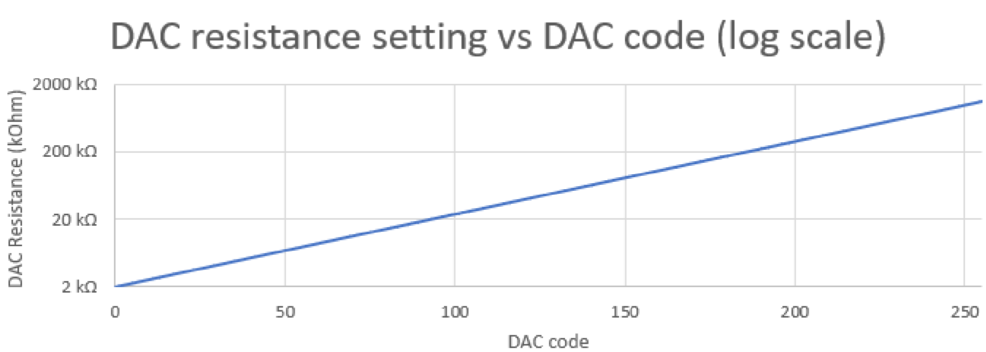


Figure 6: DAC Resistance Setting vs. Code

The Flux time setting can be set to vary inversely with the V_{IN} voltage or to be fixed and not change as V_{IN} changes. A brief explanation is included below for how the inversely proportional to V_{IN} mode can achieve a constant peak inductor current and near constant laser peak current level.

Flux Time, Cres Charge and Fire Time Control

The Schottky Anode Voltage Shown in *Figure 7* (green waveform) is pulled to Ground during the Fluxing time as shown in *Figure 2*. The voltage across the inductor with the Schottky Anode at ground is thus fixed to $\mathbf{V_{IN}}$ – 0V = $\mathbf{V_{IN}}$. Using *Equation 4* and knowing that the inductor current at the beginning of the Fluxing time is always zero, we can define the equation components as V= $\mathbf{V_{IN}}$, L=inductor value dt=Fluxing time. By rearranging the equation, we can solve for the inductor current (I_{Lpeak}) at the end of the Fluxing period.

Equation 4: $i_L = \frac{V}{L}\int_0^{T_{flux}} dt$

Equation 5: $I_{Lpeak} = V_{in} * \frac{T_{flux}}{L}$

The default setting for the fluxing time control of the SL2002 uses the equation above to maintain a constant peak inductor current at the end of the Fluxing time (I_{Lpeak}) by changing the Fluxing time inversely proportional to changes in the $\mathbf{V_{IN}}$ voltage.

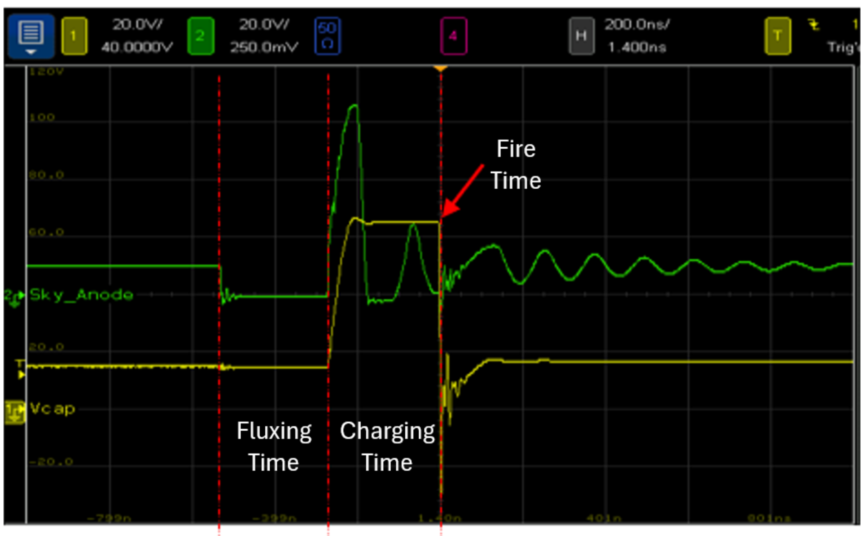


Figure 7: Firing Sequence

The $\mathbf{V_{IN}}$ dependent Flux time can be set for an average $\mathbf{V_{IN}}$ voltage of 5V. The Flux time will automatically change inversely to $\mathbf{V_{IN}}$ over a $\mathbf{V_{IN}}$ range of 2.8V to 6V. If $\mathbf{V_{IN}}$ strays beyond the range settings, there is a risk that Flux time will no longer automatically change to correct for the changes in $\mathbf{V_{IN}}$ allowing the inductor current peak to also change in proportion to $\mathbf{V_{IN}}$. The graph in *Figure 8* shows the inversely proportional behavior of the Flux Time to the $\mathbf{V_{IN}}$ voltage. The orange curve has longer Flux time due to the lower $\mathbf{V_{IN}}$ voltage of 2.8V while the red curve has shorter Flux time due to the higher $\mathbf{V_{IN}}$ voltage of 6V.

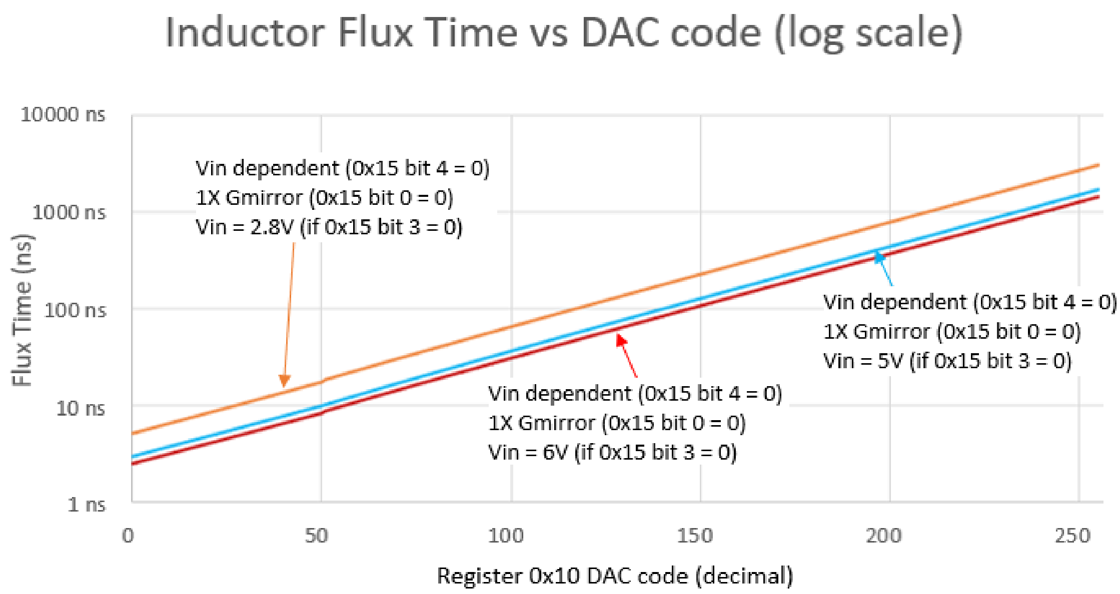


Figure 8: Flux Time vs. DAC Code (Vin Dependent)

The Flux time varies inversely with the $\mathbf{V_{IN}}$ voltage and as a result the peak inductor current (IL_peak) will be constant for a given value of inductance is predicted by *Equation 5.*
The graph in *Figure 9* below shows the Inductor Peak Current with Gmirror=1 & 440nH inductor or Gmirror=2 & 220nH inductor.

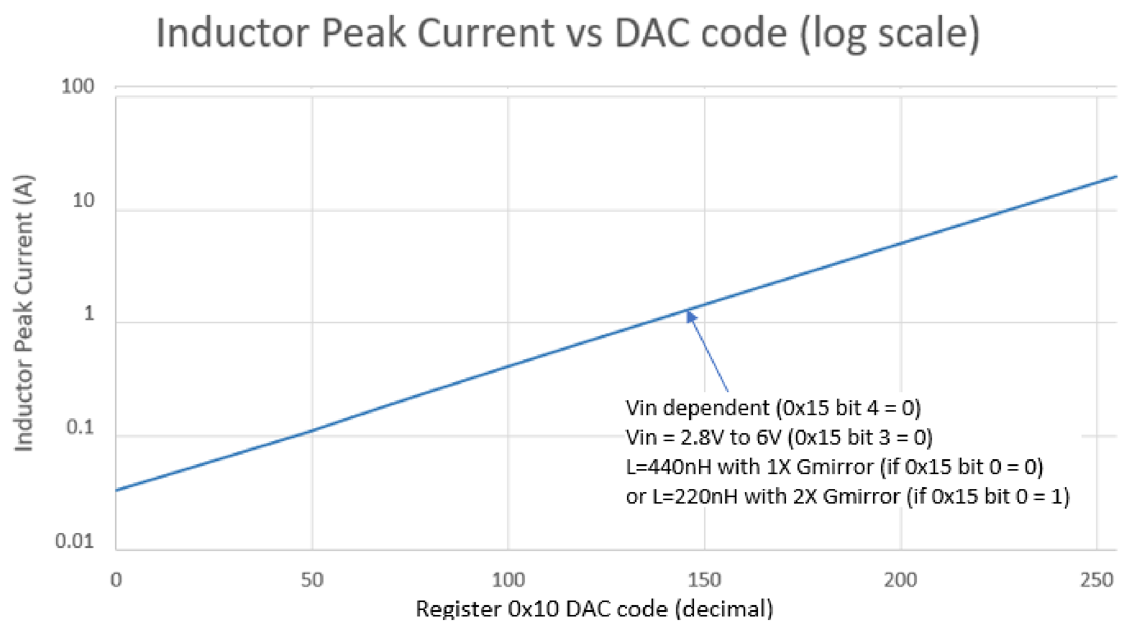


Figure 9: Peak Current vs. DAC Code (V_{IN} Dependent)

For smaller values of inductors, a 2x Gmirror setting is available. This mode approximately doubles the current into the capacitor of which decreases Flux Time for a given DAC setting by a factor of ~1.8. The I²C interface can be used to adaptively change the DAC resistor setting which varies the Inductor Flux time (Tflux). This will change the inductor peak current (IL_peak) which in turn will increase or decrease the voltage of the resonant capacitor (Cres) and the current through the laser diode when it is fired. For customers who want to adaptively change the peak inductor current (IL_peak), but do not want to use the I²C interface, an option is included where the part does not automatically vary the

Flux time (Tflux) as V_{IN} varies. With this option, the customer can vary V_{IN} to change the inductor peak current (IL_peak) according to *Equation 5*.

The graph in *Figure 10* below shows the inductor flux time (Tflux) for the mode where the Flux time is independent of V_{IN} for the 1x and 2x current mirror gain (G_{mirror}) settings and for an option to change the Vref voltage from 1.25V down to ½ of that value (0.625V).

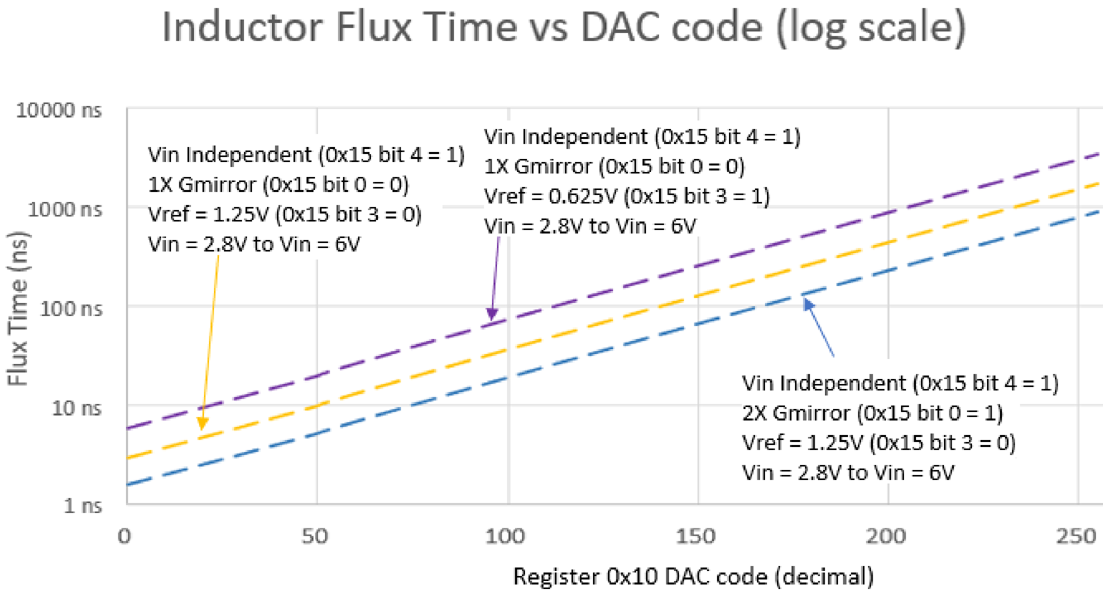


Figure 10: Flux Time Independent upon V_{IN}

The Flux time does not change as the V_{IN} voltage changes, the corresponding peak inductor current (IL_peak) will change for a given value of inductance per the Graph in *Figure 11.* This graph shows the Inductor Peak Current at different values of V_{IN}. Note that the options for the gain setting of G_{mirror} and the voltage setting of Vref allow for the same peak current to be achieves with 3 different inductor values.

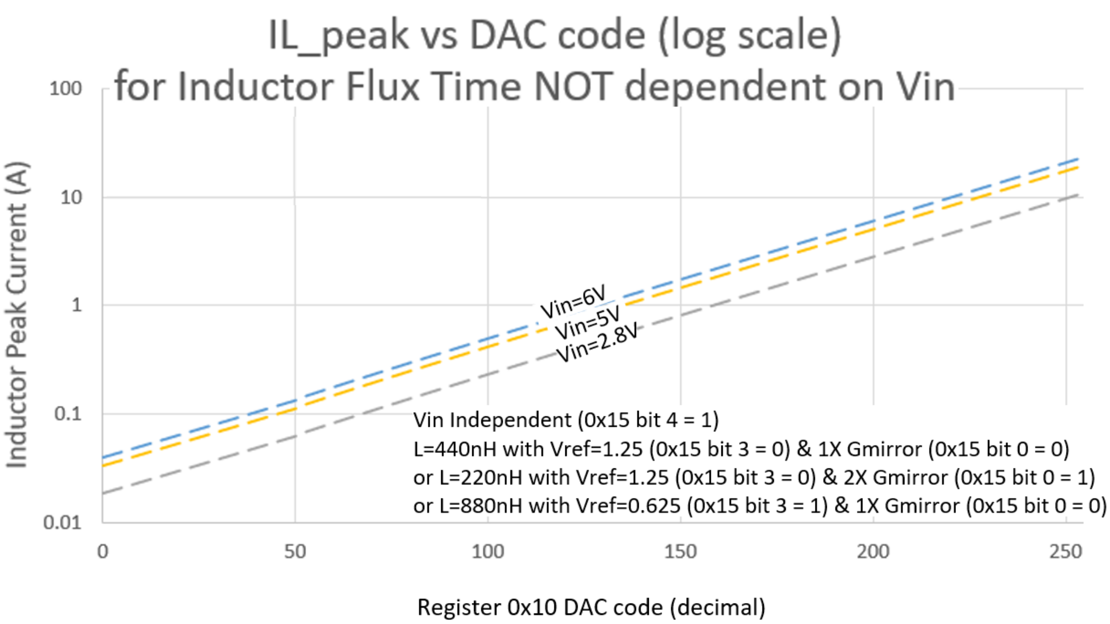


Figure 11: Peak Current Independent upon V_{IN}

For the Flux Time Dependent upon V_{IN} mode, the DAC range can be modified by selecting 1X or 2X Gmirror setting via Register 0x16 bit 0 as shown in *Figure 8* and *Figure 9*. For the Flux Time Independent upon V_{IN} mode, the DAC range can be modified by selecting Vref = 1.25V or 0.625V via Register 0x16 bit 3 and by selecting 1X or 2X Gmirror setting via Register 0x16 bit 0 as shown in *Table 3* and in *Figures 10* and *11*.

Decimal Code	00x15 bit3=0 00x15 bit0=1	00x15 bit3=0 00x15 bit0=0	00x15 bit3=1 00x15 bit0=0
fixed Flux DAC range	low L range, Vref = 1.25V and 2X Gmirror	middle L range, Vref = 1.25V and 1X Gmirror	high L range, Vref = 0.625V and 1X Gmirror

Table 3: Flux Inductor Ranges

For timing *Mode 1* described in *Figure 3*, the Charge Time (the time between the C_{res} voltage rising and the laser firing) is set with the same formula as the Flux time; however, each charge time will be ~4ns longer than the same code setting for Flux Time, Due to internal noise, the Charge time may vary during operation to as much as 25% below the set time range. This does not affect the peak light current from the laser. *Figure 12* below shows the Charge Time verses DAC code for *Mode 1*.

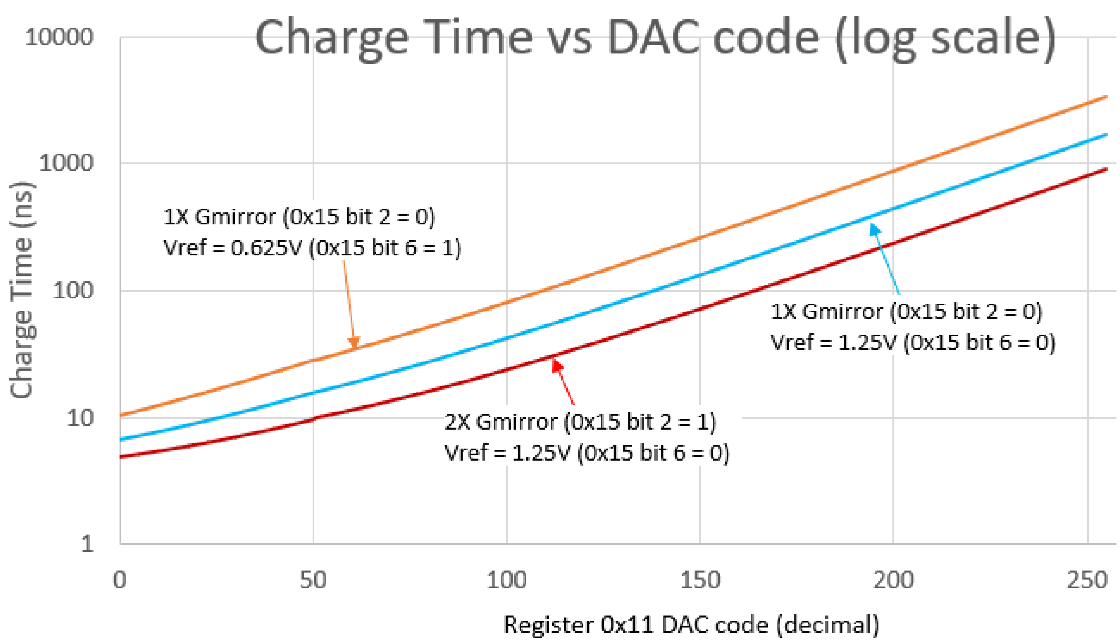


Figure 12: Charge Time verses Register 0x11 DAC code for Mode 1

For timing *Mode 2* described in *Figure 4*, the Charge Time is set via the duty cycle of the clock.
The Charge Time should be set high enough to cover the post charge blanking times for the Cres sense overvoltage and undervoltage circuitry, which is ~400ns. 1µs is a good typical setting since it is not long enough to get any noticeable voltage degradation in C_{res} after charging while also covering the C_{res} sense blanking times with sufficient margin.
The Pulse Width of the FireOUT signal can be adjusted to create a gate ON time long enough to reach peak laser current and short enough to not violate the negative voltage constraints of the laser and to avoid a 2nd pulse of light through the laser.

Figure 13 below shows the Fire Time verses DAC code for the 3 possible DAC modes.

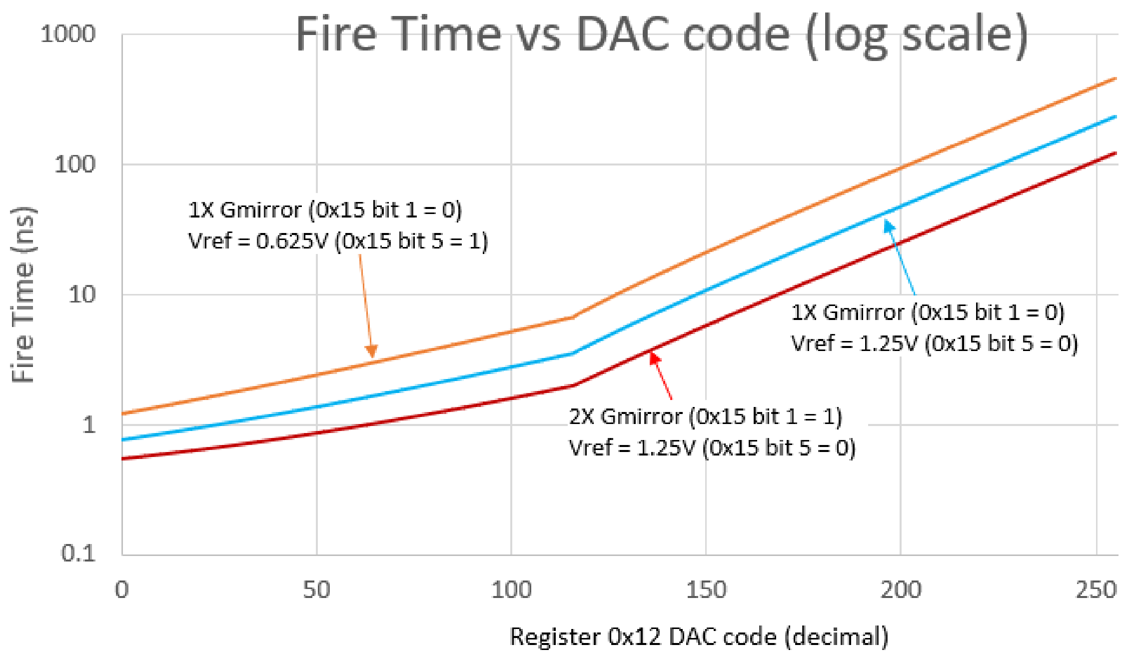


Figure 13: Fire Time verses Register 0x12 DAC code

High Level Register Map

A basic Register Map is shown below but for more detailed information please consult the SL2002 GUI Application Note.

Regmap

read/write backed by MTP	Register Bytes 0x10 to 0x16 can be read/written from/to and are loaded during start-up by 3 times programmable MTP memory.
read/write I2C only	These register Bytes can be read and written to/from via I2C but they are not associated with any nonvolatile memory addresses
read only	These bits are set internally by the SL2002 and can ONLY be read via I2C (not associated with any nonvolatile memory addresses)
read/reset status	The SL2002 will set bits of register 0x90 to one if an associated fault occurs. The user can reset any of these bits back to zero viaI2C write (not associated with any nonvolatile memory addresses)
NVM action	Writing a one to bit one or zero of register 0x8A via I2C will cause the SL2002 to perform a write or read from the non volatile memory address in register 0x8B. After completing the requested action, the SL2002 will auto clear this bit back to a zero. (not associated with any nonvolatile memory addresses)

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0
Flux Time Control	0x10	FluxTime[7]	FluxTime[6]	FluxTime[5]	FluxTime[4]	FluxTime[3]	FluxTime[2]	FluxTime[1]	FluxTime[0]
Charge Time Cntrl	0x11	ChargeTime[7]	ChargeTime[6]	ChargeTime[5]	ChargeTime[4]	ChargeTime[3]	ChargeTime[2]	ChargeTime[1]	ChargeTime[0]
Fire Time Control	0x12	FireTime[7]	FireTime[6]	FireTime[5]	FireTime[4]	FireTime[3]	FireTime[2]	FireTime[1]	FireTime[0]
Function 3	0x13	SupplyOK_VTH[1]	SupplyOK_VTH[0]	VinOV_VTH[2]	VinOV_VTH[1]	VinOV_VTH[0]	DO NOT USE	VinUV_VTH[1]	VinUV_VTH[0]
Function 4	0x14	DutyCyleMode	FluxOV_VTH[1]	FluxOV_VTH[0]	FireOV_VTH[2]	FireOV_VTH[1]	FireOV_VTH[0]	FluxUV_VTH[1]	FluxUV_VTH[0]
Function 5	0x15	DigSoftRset	TChargeRef	TFireRef	TFluxRef[1]	TFluxRef[0]	TCharge2x	TFire2x	TFlux2x
Function 6	0x16	FluxOVBehavior[1]	FluxOVBehavior[0]	CresUVBehavior	FireUV_VTH[1]	FireUV_VTH[0]	DontSkip1stFlux	i2c_address[1]	i2c_address[0]
nvm_ctrl	0x8A	vpp_mode	keep these 3 bits at 000			vpp_req	wr_en	wr	rd
nvm_addr	0x8B	nvm_addr[7:0]							
nvm_wdata	0x8C	nvm_wdata[7:0]							
nvm_rdata	0x8D	nvm_rdata[7:0]							
status_fault	0x90	Over Temp	VinOV	VinUV	CresUV pre-Charge	CresOV pre Charge	CresOV post Charge	CresUV post Charge	SupplyOK Fault

Table 4: Register Map

Non Volatile Memory (NVM)

In addition to real time I²C programmability during operation, registers 0x10 though 0x16 above can also be set via SL2002's three-time programmable Multiple-Time-Programmable (MTP) ROM, which will be loaded to those registers when the part starts-up. The SL2002 also contains 219 additional One-Time-Programmable (OTP) Bytes in memory addresses (0x17-0x5F and 0x67-0xAF and 0xB7- 0xFF) that users can use as they wish. These are additional Bytes of memory that have no direct impact on product operation and can be loaded with any information, for example board or laser specific information that a microcontroller could use to modify register settings during operation due to temperature or other variations.

One example for use of the 219 Bytes of OTP would be to store board specific information about the optimal Flux Time Control (Register 0x10) codes for various laser temperatures and/or other environmental variants to achieve one or several desired Light power profiles. During operation, the temperature could then be sensed near to the laser, and the code could then be read back via I²C for the memory address associated with that temperature, such that the code in that memory address could then be written via I²C to register 0x10 to modify the Flux Timing.

Protection and Fault information

The SL2002 offers several highly programmable fault options and settings. A summary of the Fault Options with more specific information about each option is described in this section.

Mask Faults

(Register 0x01)

The SL2002 can be programmed via One Time Programmable ROM or via I2C to mask or react to any of the faults. The GUI settings for the Fault Enable Register (0x01) are shown in *Figure 14*. Whether or not the fault is masked, its corresponding bit in the Fault Status Register (0x90) will be set to a 1 to indicate that the fault has occurred. The GUI settings for the Fault Status Register (0x90) are shown in *Figure 15*.

Hiccup Mode (Default):

Register 0x02 bits 7:0 set to 0)

When a Fault is registered in the Digital circuitry, the SL2002 will stop immediately and set both the **FluxOUT** and **FireOUT** pins to low (zero V) for 28ms. After 28ms, the SL2002 will check whether the fault is still present. If the fault is still present, the SL2002 will continue holding both **FluxOUT** and **FireOUT** low and wait another 28ms before checking the fault status again. Once the fault is no longer present (checking every 28ms), the SL2002 will immediately begin driving both the **FluxOUT** and **FireOUT** pins again per the previous clock and timing settings.

Fault Latch Off Mode:

Register 0x02 bits 7:0 set to 1)

The SL2002 has the option over the I^{2}C interface to not “hiccup” but rather to “latch off” when any of the selected faults are registered. If the SL2002 does latch-off due to a fault, then the **FluxOUT** and **FireOUT** pins will be held low until either 1 of the 2 events occurs:

1. The DigSoftReset bit (bit 7 of register 0X15) is set to a 1 via the I^{2}C interface (this bit will be reset back to 0 automatically upon reset)
2. The **AV$_{DD}$** voltage is brought below 1V, then brought back up above 3V

Upon either event 1 or 2 occurring, the SL2002 registers will go through its start-up sequence such that all registers will be set according to the NVM settings and then check whether any faults exist before beginning to drive the **FluxOUT** and **FireOUT** pins again.

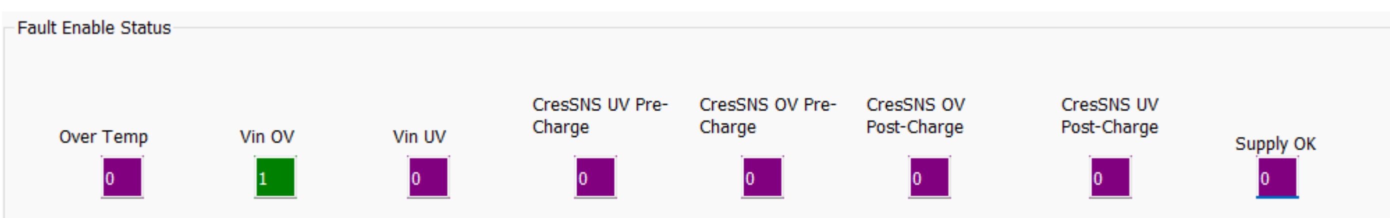


Figure 14: Fault Enable Register – OV is enabled at startup to prevent component damage

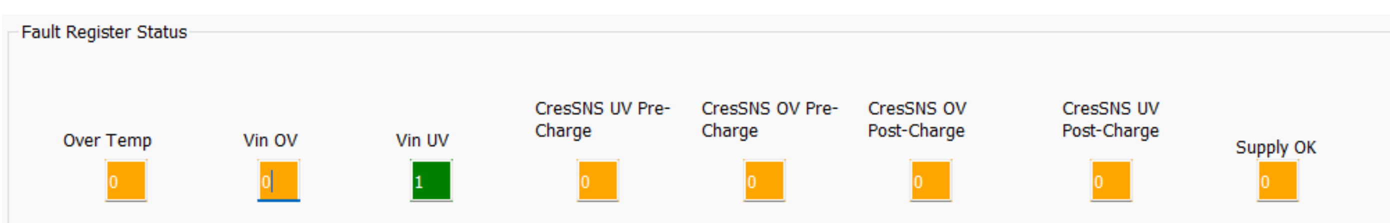


Figure 15: Fault Status Register – an example of a Vin UV fault

Device Fault Behaviour

The action that the SL2002 takes when a fault is detected is described in *Table 5*. **Note that the default setting for all faults except for V_{IN} overvoltage is NOT enabled in digital (Register 0x01).** So, to perform the action shown in Table 6, the corresponding bit in Register 0x01 will have to be written to a value of 1.

Fault Condition	Action (when SL2002 is configurated to enable each fault)
V_{DD} voltage is too low	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit0)
Cres voltage After Charging is too low	- Prevent FluxOUT and FireOUT pins from going high after fault is present for 4 consecutive cycles - Assert Fault Status bit (Register 0x90 bit1)
Cres voltage After Charging is too high	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit2)
Cres voltage Before Charging is too high	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit3)
Cres voltage Before Charging is too low	- Prevent FluxOUT and FireOUT pins from going high - Assert Fault Status bit (Register 0x90 bit4)
V_{IN} voltage is too low	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit5)
V_{IN} voltage is too high	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit6)
Over Temperature	- Prevent FluxOUT and FireOUT pins from going high immediately - Assert Fault Status bit (Register 0x90 bit7)

Table 5: SL2002 Fault Conditions and Action

Starting from the bottom left corner of *Figure 16* below upon **AV_{DD}** rising above a voltage of approximately 2.5V, the part will wait approximately 100µs and then clear the reset for the internal Digital Engine and begin the startup fault checking. The first fault to be checked is over temperature protection, which has a typical rising threshold of approximately 140C. Per the Electrical Characteristics section, the rising threshold will always be higher than 125C and the falling threshold will be approximately 20C below the rising threshold. If an over temperature protection fault is triggered, the SL2002 will wait until either the fault is no longer triggered or 28ms has passed, then continue through the rest of the startup sequence. After waiting approximately 50µs, the CresUV_pre, Supply OK and **V_{IN}** UV/OV faults will all be checked. If any of the CresUV_pre or **V_{IN}** UV/OV faults are present, their corresponding bit in the Fault Status Register (0x90) will be set to 1, then (only if the corresponding Fault Enable bit in Register 0x01 is set to 1 and the Supply OK Fault is not present) the SL2002 will immediately move to FAULT mode. If the Supply OK Fault is present, SL2002 will wait until the Supply OK Fault is no longer present, then proceed to normal operation (after a programmable delay). In normal operation, all Faults will be continuously monitored. If any Fault occurs, its corresponding bit in the Fault Status Register (0x90) will be set to 1, then (only if that Fault's corresponding bit in the Fault Enable Register 0x01 is set to 1) the SL2002 will enter FAULT mode. If the SL2002 enters fault mode and Hiccup Mode is selected for the fault that has occurred (Register 0x02 corresponding bit is set to 0), then the SL2002 will hold the **FluxOUT** and **FireOUT** pins low, wait for approximately 28ms, and re-enter Normal Operation. If the SL2002 enters fault mode and Shutdown Mode is selected for the fault that has occurred (Register 0x02 corresponding bit is set to 1), then the SL2002 will enter Latch Off mode where the **FluxOUT** and **FireOUT** pins will be held low. The SL2002 can be restarted from Latch Off mode by either bringing **AV_{DD}** below approximately 2V or by writing the DigSoftReset bit to 1 (Reg 0x15 bit 7).
In *Figure 16*, the Digital Reset Clear state that is entered immediately after Startup or upon exit from Latch Off will reset all bits of the Fault Status Register (0x90) to 0. For all other times during operation, the Fault Status Register bits are "sticky", meaning that if any bit is set to 1 due to its corresponding fault occurring, then it will stay as a 1 unless the user changes it back to a 0 via an I2C write.

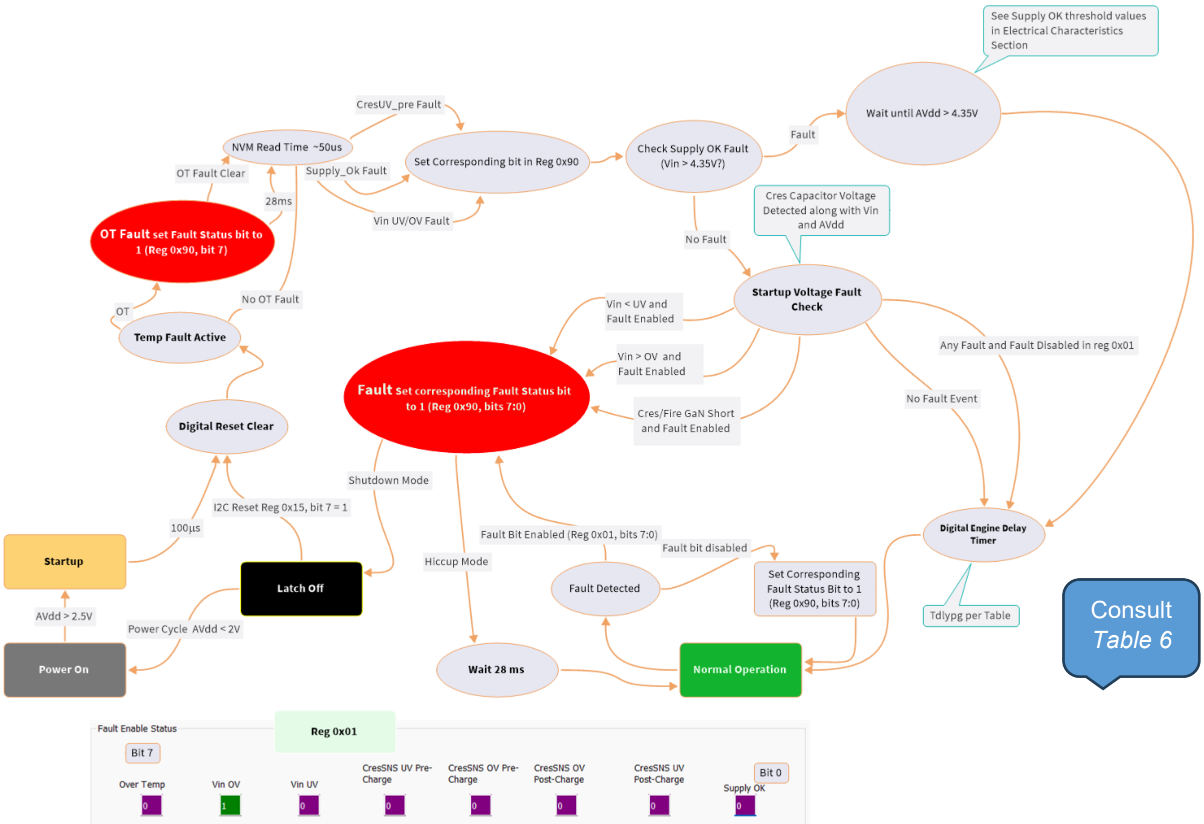


Figure 16: State Diagram of Operation and Fault Behavior

To avoid getting a SupplyOK fault flag in the Fault Status register (0x90) during startup, the **AV_{DD}** slew rate needs to be fast enough so that after **AV_{DD}** crosses 2.5V, within 100us, **AV_{DD}** will reach 4.5V. The slew rate to prevent a SupplyOK fault flag can be set by *Equation 6* below:

Equation 6: $AVdd\ Slew\ rate > \frac{4.5V-2.5V}{100\mu s} = \frac{2V}{100\mu s}$

If a **V_{IN}** UV Fault occurs and is enabled (Register 0x01 bit 5 set to 1), the SL2002 will enter FAULT mode and either Hiccup (wait 28ms to enter Normal Operation) or Latch Off. To prevent this from happening during startup, 3 options are available:

1) the **V_{IN}** UV Fault can be disabled via nonvolatile memory (set Register 0x01 bit 5 to 0)

2) the **V_{IN}** supply can be ramped above the **V_{IN}** UV threshold voltage before the **AV_{DD}** supply starts ramping from zero Volts

3) *Equation 7* below can be met

Equation 7: $V_{IN}\ slew\ rate\ to\ prevent\ UV\ during\ startup > \frac{2.5V}{\frac{2V}{SlewRate\_AVdd} + 150\mu s + Tdlypg}$

The Tdlypg time is programmable per *Table 6*.

For example, in order to meet *Equation 7* with separate **V_{IN}** and **AV_{DD}** supplies starting to ramp from zero Volts at the same time with a Tdlypg setting of 888µs (Register 0x00 bits 5:4 = 11), **AV_{DD}** slew rate of 1V/ms and **V_{IN}** UV rising threshold of 2.5V (Register 0x13 bits 1:0 = 00), the **V_{IN}** slew rate would need to be greater than 2.5V / (2V/1000V/s + 150µs + 888µs) = 0.65 V/ms.

If **V_{IN}** and **AV_{DD}** are operated from the same supply, then the slew rate for **V_{IN}** and **AV_{DD}** are the same and *Equation 7* simplifies to *Equation 8* below:

Equation 8: $V_{IN}\ \&\ V_{DD}\ (from\ same\ supply)\ slew\ rate\ to\ prevent\ UV\ during\ startup > \frac{0.5V}{150\mu s + Tdlypg}$

For example, in order to meet *Equation 8* with a single power supply driving both **V_{IN}** and **AV_{DD}** with a Tdlypg setting of 888µs (Register 0x00 bits 5:4 = 11), the **V_{IN}** & **AV_{DD}** (from same supply) slew rate would need to be greater than (0.5V) / (150µs + 888µs) = 0.48 V/ms.

bit5	bit4	Register 0x00, bits 5:4, FuseTime
0	0	Tdlypg = 18us
0	1	Tdlypg = 89us
1	0	Tdlypg = 355us
1	1	Tdlypg = 888us

Table 6: Tdlypg programmable delays for OTP read mode to full Function mode.

In a typical application, a charge pump can be used to convert a low voltage **V_{IN}** supply into the 5V needed for Vdd of the SL2002. Per *Figure 17* below, when the **V_{IN}** supply (yellow) is ramping up, Vdd (green) will follow at about a diode below **V_{IN}** until the voltage at which the charge pump begins to function (~2.3V in *Figure 17*) and then rise above **V_{IN}** toward the 5V target. Depending on the Charge Pump's output capability, Vdd might ramp up under different slew rates. When the slew rate is lower than 2V/100us (per *Equation 6*), the SL2002 will activate a Vdd supply UV fault during startup. Per *Figure 16*, this will set the Supply OK bit 0 of the Fault Status Register (0x90) to a value of 1 and gate the internal startup logic to prevent IC from starting operation until Vdd has reached 4.35V. As soon as Vdd reaches 4.35V, the IC will enter full functional mode with the programmable delay of Table 6 (assuming no other fault condition is occurring).

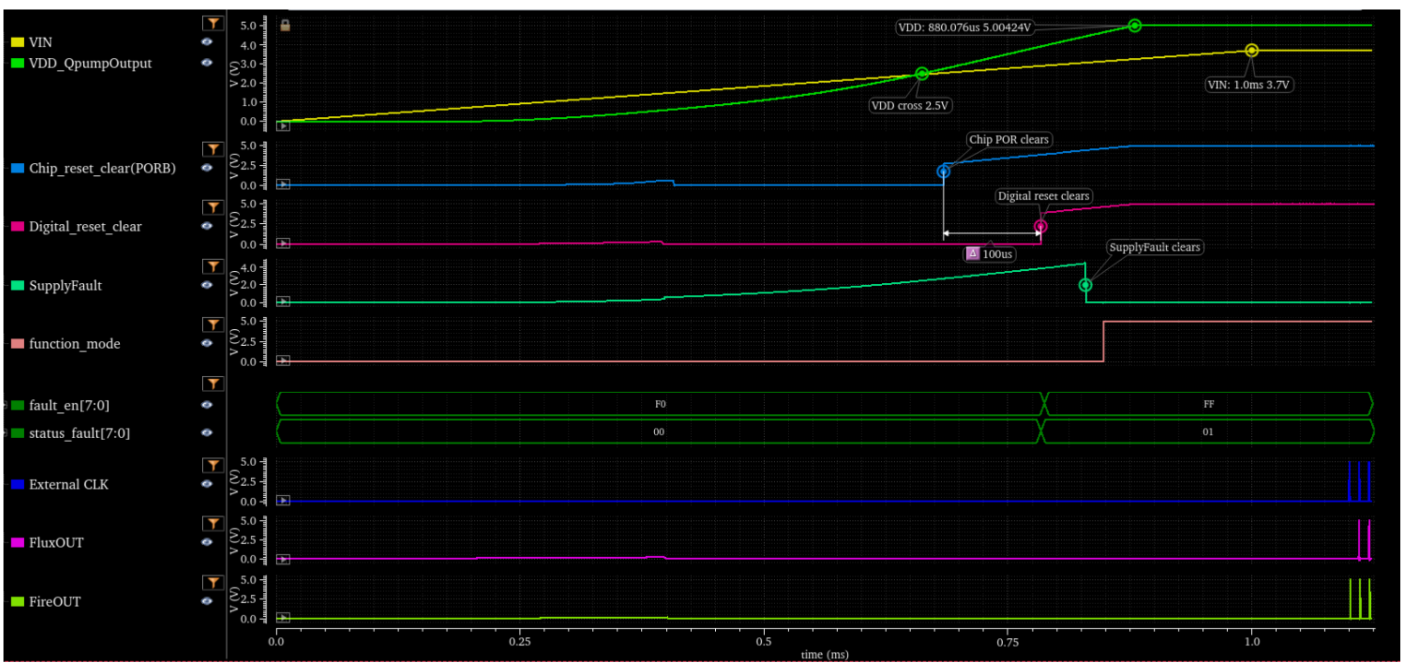


Figure 17: Startup Waveforms where V_{DD} ramps slowly from the charge pump

Figure 18 shows the operation of the programmable delay time (from *Table 6*) before entering full functional mode. Also note from *Figure 18* that the CresUV pre-charge feature is not enabled until Vin is above 4.5V in order to prevent fault mis-tripping.

Figure 18: Start-up waveforms for OTPready, FunctionMode and the C_{res}SNS valid signal

V_{IN} UV and OV Faults

The Fault Threshold for V_{IN} Undervoltage is a typical value of 2.5V and the V_{IN} Overvoltage Fault threshold is a typical value of 6.5V. If the V_{IN} UV fault is disabled, the SL2002 will continue to operate even with V_{IN} at zero. The undervoltage Fault is still Monitored to give an indication of V_{IN} falling below the intended supply voltage range.

Cres Related Faults

The **Cres_SNS** pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in *Figure 21*. Fault thresholds are shown in the Electrical Characteristics section for an external 6.8MΩ resistor; however, a formula (*Equation 1*) is included in the Detailed Pin Descriptions section that is valid for external resistor values between 5MΩ and 8MΩ.
Please ensure that the external resistor can support the maximum voltage that will be seen on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points.

Figure 19 below, shows the Cres fault detection window for one operation cycle using timing mode 1.
450ns of blanking time is included after **FluxOut** goes low (for Cres post charge OV and UV fault checking) to ensure that the Cres sense circuits do not false trip due to the noise of a transient event. The valid Cres post charge OV and UV window will be 450ns after the **FluxOut** goes low and before the Charge Time ends (the high time of the light blue waveform). It is important to set the Charge Time to be longer than the blanking time with some margin. Otherwise, the detection will never be activated.

Similarly, for **Cres** pre charge OV and UV fault, the valid detection window will be 450ns after the **FireOUT** goes low and before an internal 10us timer expires (the high time of the dark blue waveform). The 10µs timer is included so that a normal amount of leakage on the VCAP voltage for a long amount of time (much greater than 10µs) will not incorrectly flag as a Cres pre charge UV fault.

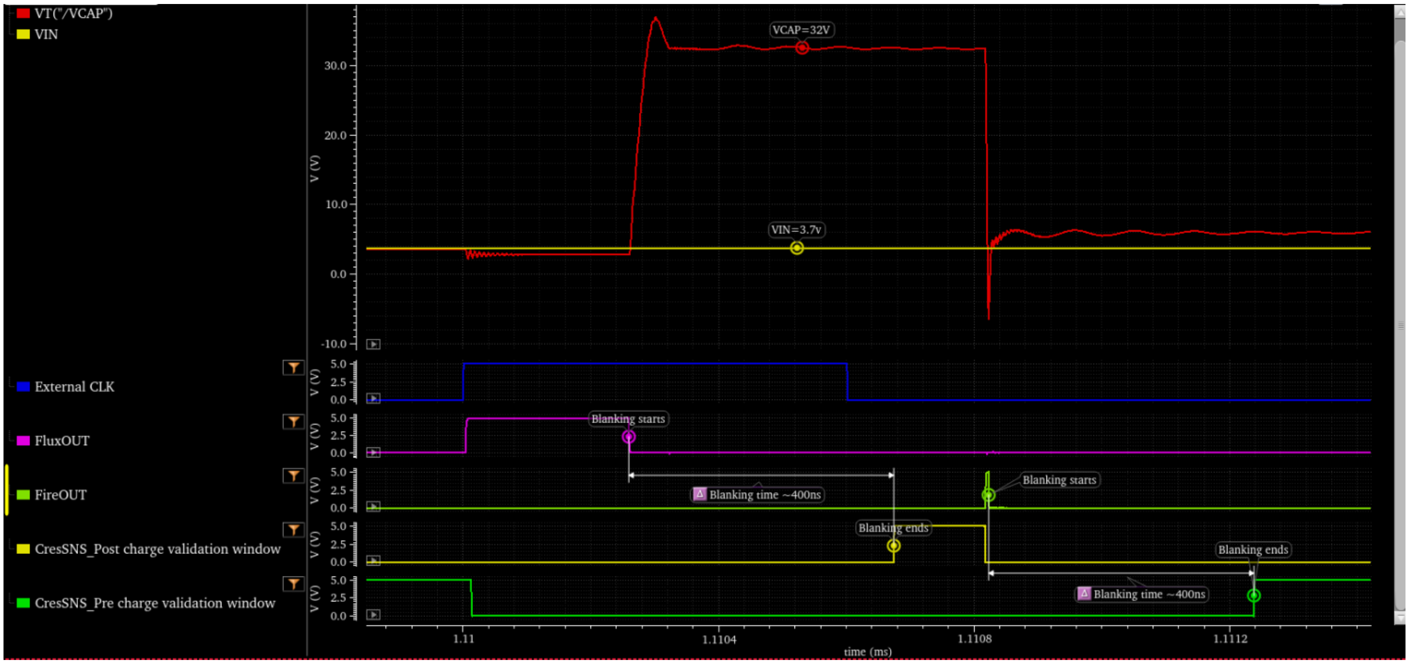


Figure 19: Fluxing and Firing Timing

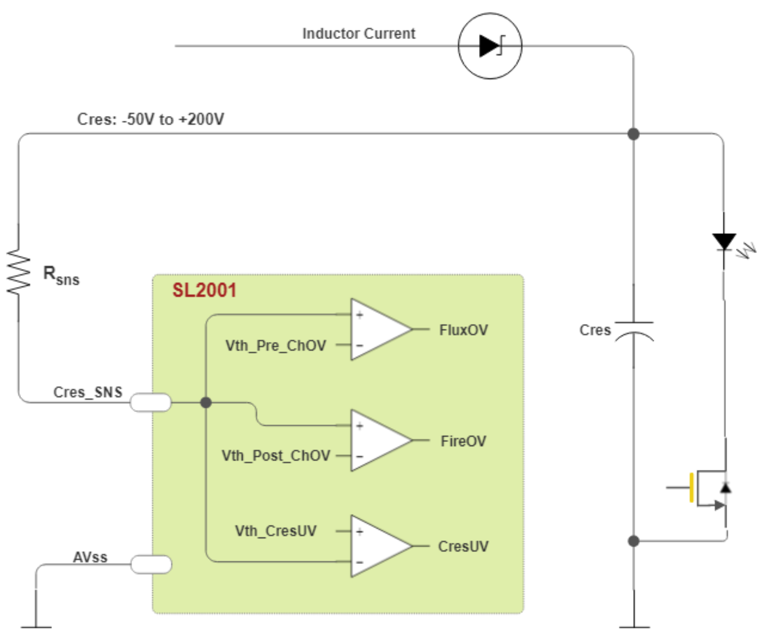


Figure 20: SL2002 Fault Diagram

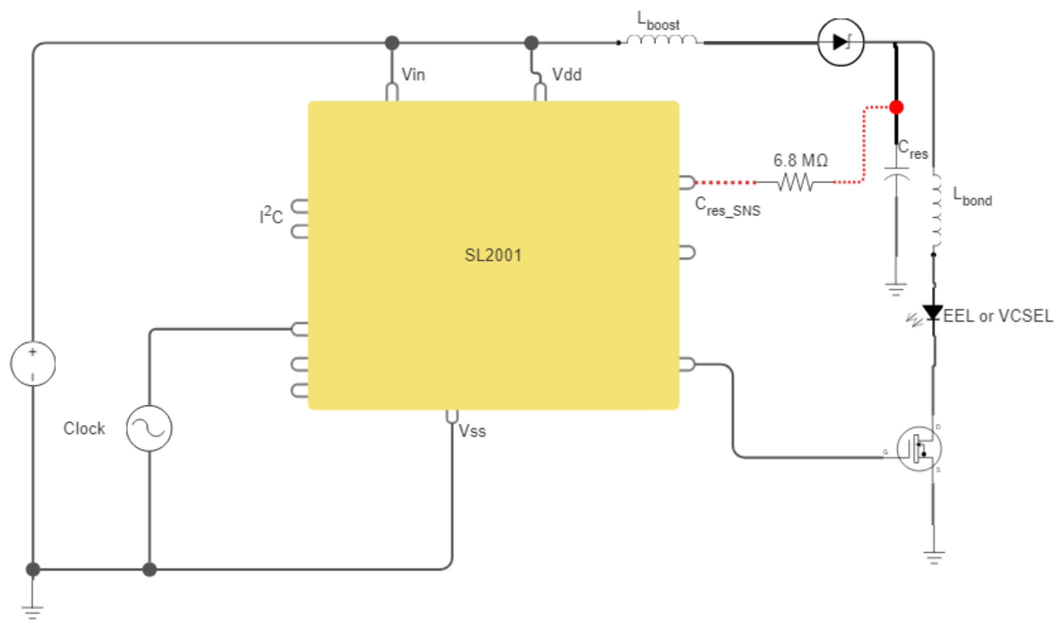


Figure 21: Cres Sense from the Anode Side

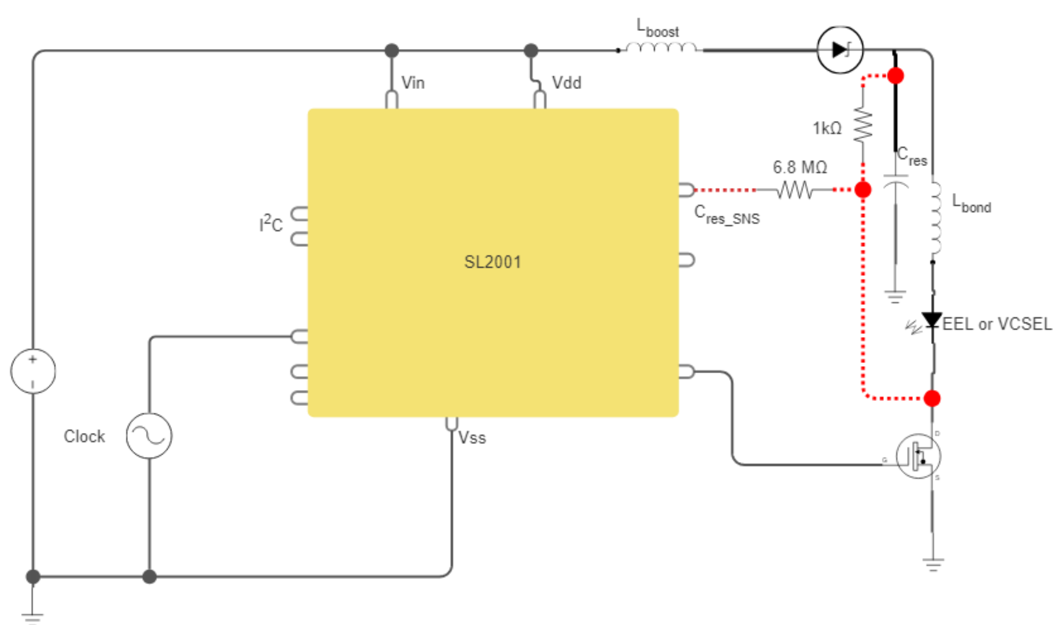


Figure 22: Cres Sense from the Cathode

It is also possible to sense at the Laser cathode as per *Figure 22*. In an application where short detection of Laser Firing GaN FET is critical, using a cathode sensing scheme will ensure a more accurate short circuit detection. For example, in *Figure 21*, when a weak short circuit occurs across the Laser firing GaN FET, it might only produce 100mA of current going through the Schottky diode. Therefore, the voltage drop across the Schottky diode isn't significant enough to be detected as a Cres UV pre-charge fault. This can cause the Laser diode to continue to emit light without being properly controlled. The Laser cathode sensing scheme ensures more accurate short circuit detection because of the additional voltage drop across the laser diode. It is recommended to add a resistor across the laser diode, as shown in *Figure 22*. This enables the Laser cathode to settle faster and sync with the anode after the laser firing event. *Figure 23* shows an example waveform without any resistor between Laser Anode and Cathode. In this case the Cathode voltage doesn't reflect the true Anode (VCAP node) voltage before or after Laser fired. The resistor value should be chosen based on the value of parasitic capacitance in the Laser firing path (including Laser Firing GaN Cds and PCB parasitics), so that 3*RC time constant value is <300ns (after 3*RC time constants, the resistor has reached 95% of its final value). This ensures that the CresSNS input signal settles before the internal blanking time (for noise filtering) expires. *Figure 24* and *Figure 25* show the settling times for 1KΩ and 180Ω resistor values using the SLE2001-E01 evaluation board (modified for cathode sensing). For that board, the 1kΩ resistor provides a 3*RC time constant of ~1.26μs while the 180Ω resistor provides a 3*RC time constant of ~240ns. For that board, we recommend a resistor value that is less than or equal to 225Ω.

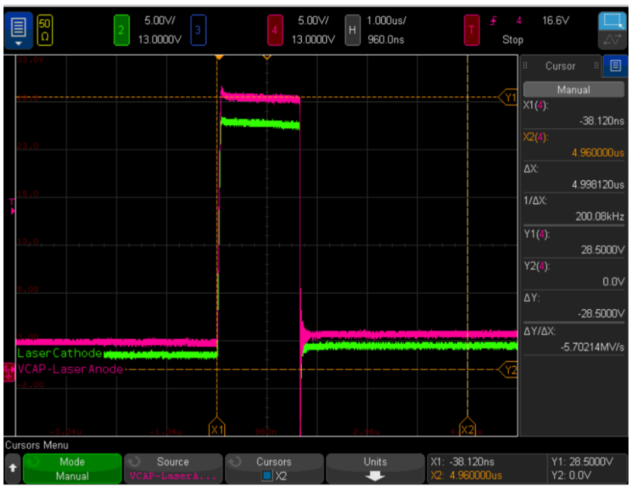


Figure 23: Laser Anode vs. Cathode without any resistor across Laser during operation

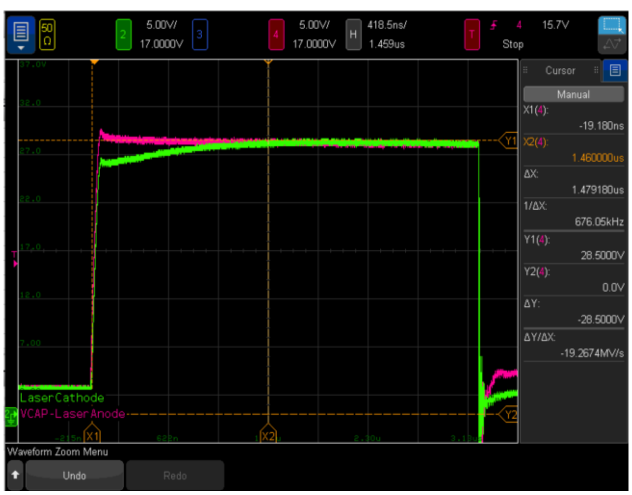


Figure 24: Laser Anode vs. Cathode with 1K ohm RES across Laser during operation

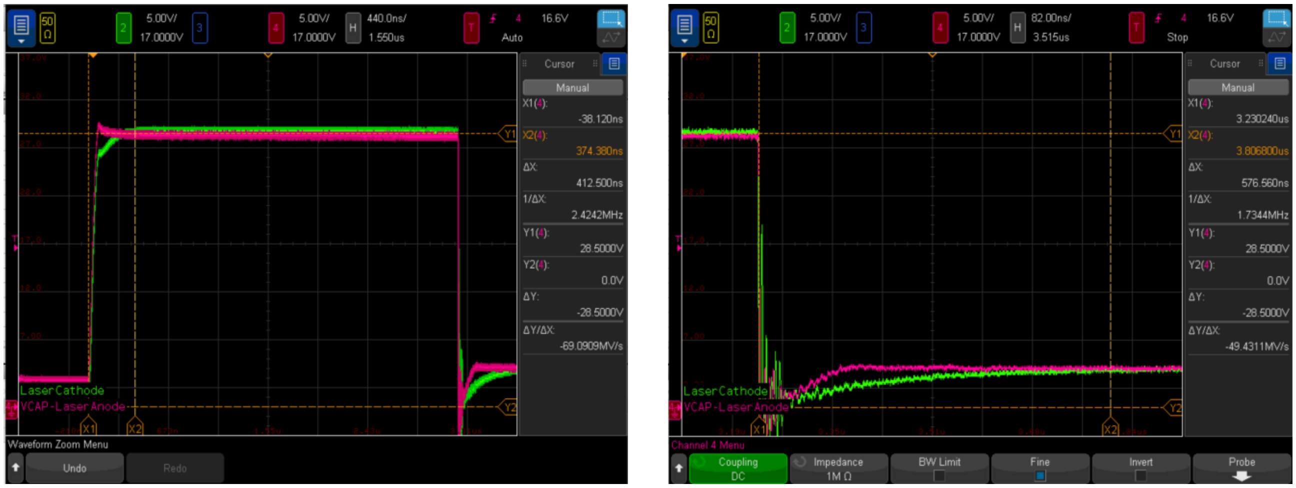


Figure 25: Laser Anode vs. Cathode with 180 ohm RES across Laser during operation

Eye Safety

During the IC startup sequence, if **V$_{DD}$** and **V$_{IN}$** are biased separately and **V$_{DD}$** reaches 4.5V before **V$_{IN}$**, the SL2002 will be able to capture the short circuit between Laser firing GaN FET source and drain. The reaction to this fault condition can be programmed to force the SL2002 to turn on the Fluxing GaN FET which directs current from **V$_{IN}$** to ground instead of going through the laser. This prevents the laser from emitting light until the SL2002 goes through a power cycle or is digitally reset via I^{2}C. *Figure 26* gives an example waveform using this cathode sensing scheme. In this example, the system starts up and encounters a short circuit between the Laser cathode and ground (source and drain of the Laser firing GaN FET). **This protection scheme is only available when V$_{IN}$ is above 4.5V** to ensure accuracy and prevent false tripping. When the **V$_{IN}$** supply is ramping up, Laser diode will start to conduct current via the short circuit. Once the **V$_{IN}$** is above 4.5V, the short circuit is detected, and protection is activated. To ensure the laser will stop emitting light, Register 0x05 bit 7 can be set to a 1 to latch the **FluxOUT** pin output to a high state and steer the **V$_{IN}$** current away from the laser to the ground path.

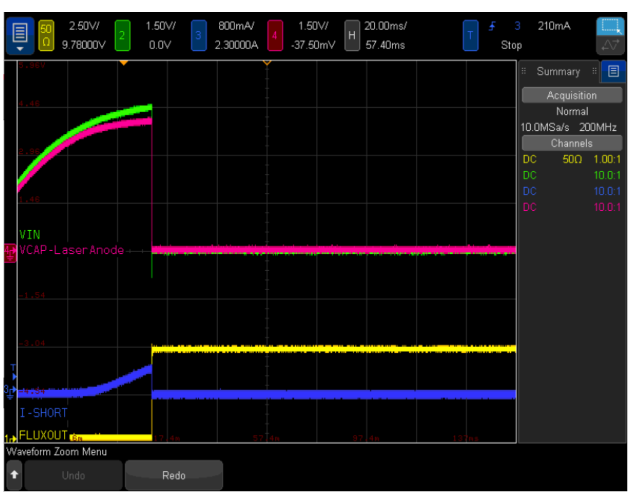


Figure 26: Laser firing GaNFET Short protection engaged after V$_{DD}$ bias in place and during V$_{IN}$ ramping up (cathode sense)

In applications where **V$_{DD}$** and **V$_{IN}$** supplies are combined, the short circuit protection can still be triggered as shown in *Figure 27*. However, because **V$_{DD}$** and **V$_{IN}$** are sharing the same supply, if the Fluxing GaN is programmed to latch on due to a Cres UV fault, it may deplete **V_{DD}** and cause IC to go into power on reset and turn off the Flux GaN FET. If **V_{IN}** and **V_{DD}** try to rise again, a repeat of these events will occur if the short is still present. An input power fuse is recommended in this case.

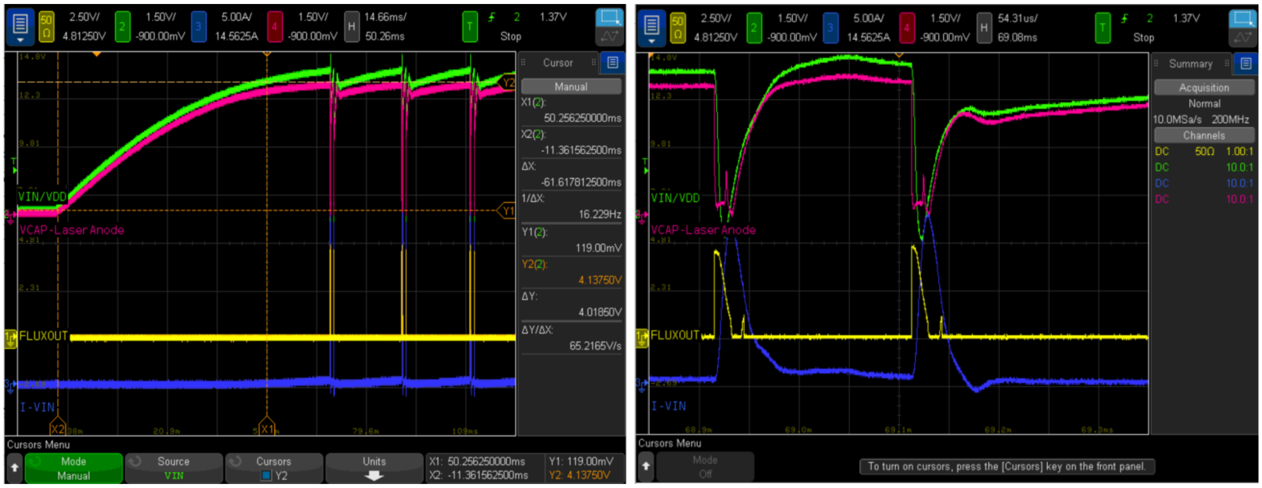


Figure 27: Laser firing GaNFET Short Circuit Protection engaged when V_{IN} &V_{DD} are biased from the same supply and zoom in view (cathode sense)

During normal operation, a short circuit between the Laser cathode and ground can also be detected by the IC. An example of this occurrence is depicted in *Figure 28.* The short circuit for the waveforms of *Figures 27 & 28* occur with a 1KHz repetition rate and is sensed using the laser cathode sensing scheme.

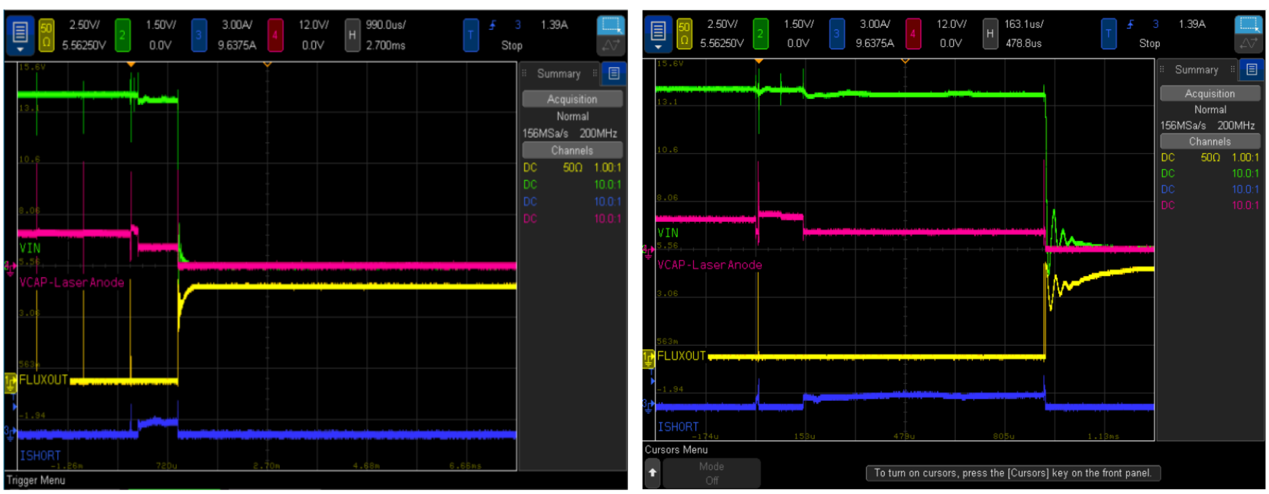


Figure 28: Laser firing GaNFET Short Circuit Protection engaged during operation when V_{IN} &V_{DD} are biased separately and zoom in view

Reference Design

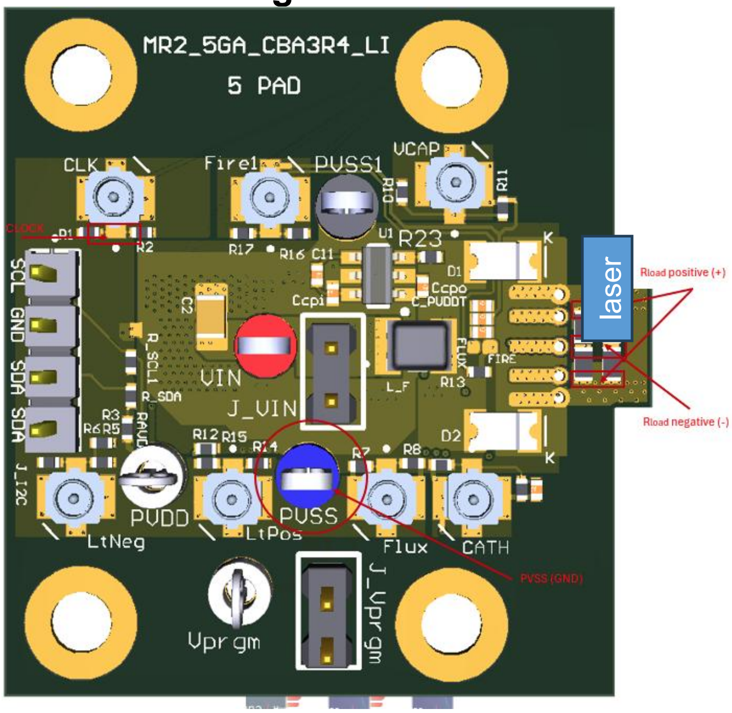
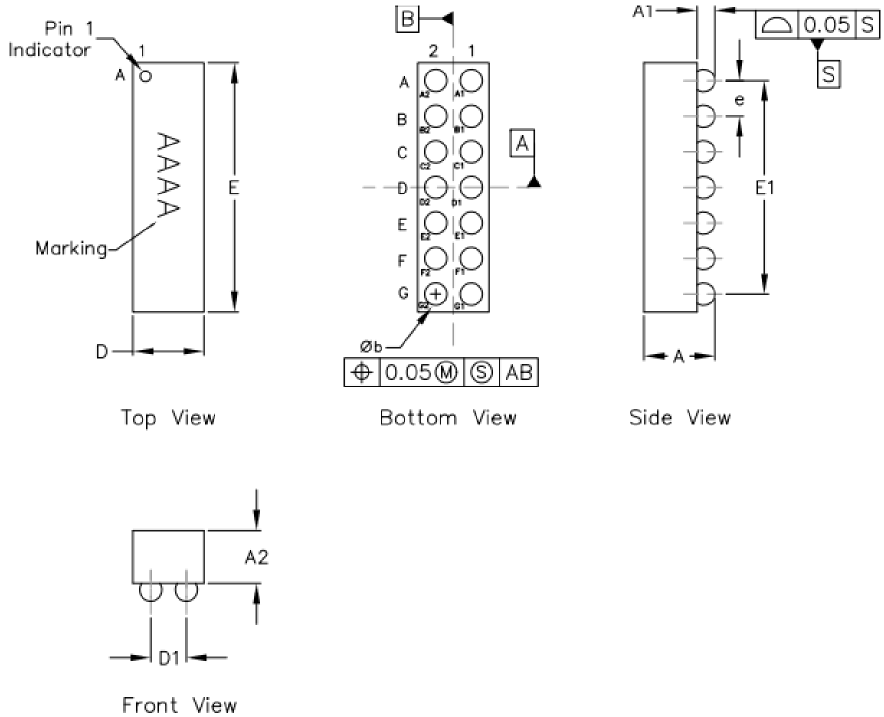


Figure 29: SL2002 Evaluation Board

Package Dimensions



COMMON DIMENSION	
SYMBOL	VALUE
A	0.995 ±0.05
A1	0.250 ±0.03
A2	0.745 REF
b	ø 0.315 ±0.03
D	1.000 ±0.025
E	3.500 ±0.025
D1	0.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC

NOTE:

1. TERMINAL PITCH IS DEFINE BY THE TERMINAL CENTER TO CENTER.
2. OUTER DIMENSION IS DEFINED BY CENTER LINES BETWEEN SCRIBE LINES
3. ALL DIMENSIONS IN MILLIMITER
4. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY
5. TOLERANCE IS ±0.02 UNLESS SPECIFIED OTHERWISE

Figure 30: Package Dimensions

Product Ordering Information

Part Number	Package	Feature	Shipping Method
SL2002A-WHS	14 Pin bumped flip chip	200W Peak Power Laser Driving System with Integrated Timing Controller, Boost Voltage Generator and Fault Protection for Battery Driven Laser Time-of-Flight Measurement Systems	2,500 pcs Tape & Reel

Revision History

Revision	Date	Author	Note
1.0	12/10/2025	AZ	GPR Release