Application Note: Utilizing SD1148 DSP Features in Radio Receivers

Overview

Silanna's ADC portfolio includes a selection of feature-rich devices that integrate DSP blocks with 12-, 14-, or 16-bit dual-channel ADCs. The DSP features include decimation, digital downconversion (DDC), and IQ mismatch correction. The SD1148 is the 14-bit member of the product family. Multiple speed-grade options are available, ranging from 40 MS/s to 250 MS/s. The 16-bit SD1150 and the 12-bit SD1146 share the same package pinout and feature set and can be used interchangeably, depending on the application's performance requirements.

This application note presents three examples of how the SD1148 can be used in a radio receiver. A major portion of the digital front-end functionality is implemented using the embedded DSP blocks, offloading processing from the FPGA.

Direct Conversion Receiver

The direct conversion (or zero IF) receiver architecture, shown in Figure 1, uses a quadrature RF-mixer that converts the RF signal directly to DC. The signal chain starts with a band select filter followed by LNA. The LO is centered on the RF signal band. The mixer has two paths, one producing the inphase (I) and the other the quadrature (Q) output signals. A quadrature LO signal with sine and cosine components is required.

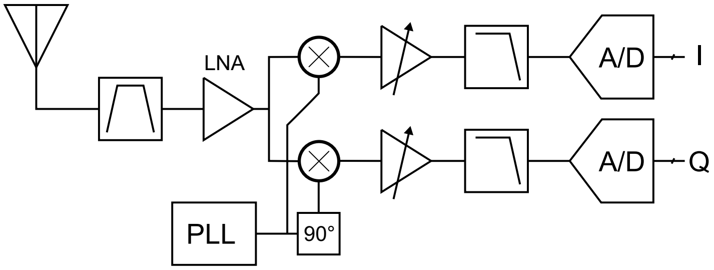

Figure 1. Simplified direct conversion receiver.

The baseband IQ signal path following the mixer typically consists of a programmable gain stage, an anti-alias filter, and finally the ADC. Many implementations include additional filtering along the signal chain and some amount of RF gain control. Channel selection can be either analog—by changing the LO frequency—or digital, in which case the LO frequency is fixed, the entire band of interest is digitized by the ADC, and digital downconversion (DDC) plus filtering are used to select the desired channel. Even in the first case, channel-select filtering is often performed partially in the digital domain.

The direct conversion architecture doesn't have to deal with image rejection as the signal is its own image. Its implementation challenges lay in dealing with LO feedthrough, 1/f noise, and gain transients. In the baseband, these issues are concentrated in the vicinity of DC and are more severe for systems using narrow channel widths, measured in kHz. They are easier to deal with when using wider channel widths and modulations that are less sensitive to low frequency content. When digital channel selection is used, placing the LO between channels largely solves these issues.

Another challenge is IQ mismatch: amplitude and phase mismatch between the I and Q components, which results in leakage between the I and Q signal paths. All baseband blocks, the mixer, and the LO contribute to this mismatch. Differential gain errors between the I and Q paths in the mixer, amplifiers, ADCs, and the filter passband gain contribute to gain mismatch. Phase mismatch is primarily caused by phase error between the LO sine and cosine components, mismatch in the filter frequency response, and, to a lesser degree, clock phase mismatch between the two ADCs. Using dual devices for the amplifier and ADC that are specifically designed for IQ applications significantly reduces the contribution from these blocks. Calibration is commonly required to suppress the mismatch to a tolerable level. For signals with modest bandwidths, a frequency-independent calibration is typically sufficient.

ADC sampling-rate selection and baseband filtering are tightly coupled. Sampled systems, including ADCs, can uniquely represent signals only over a bandwidth of Fs/2, where Fs is the ADC sampling frequency. This condition is known as the Nyquist criterion. If the ADC input contains spectral content in both the region from 0 to Fs/2 (the first Nyquist zone) and the region from Fs/2 to Fs (the second Nyquist zone), the sampling process folds frequency components from these regions onto one another. This effect is called aliasing and must be avoided. Either region can be used to place the signal of interest, but not both simultaneously.

The anti-alias filter is an analog filter placed in front of the ADC to suppress unwanted signal and noise content outside the selected Nyquist zone prior to sampling. When the signal band extends to Fs/2 – Δf, the frequencies that must be fully rejected by the filter begin at Fs/2 + Δf. This results in a transition band that is 2Δf wide. The narrower the transition band, the higher the filter order required to achieve a given attenuation. For this reason, it is advantageous to increase the ADC sampling rate beyond the theoretical minimum stated by the Nyquist criterion to relax the filter specifications. This margin is typically at least 30% and is often higher. The tradeoff is higher ADC cost and increased digital signal-processing requirements versus the cost and complexity of analog filtering. Silanna's feature-rich ADCs provide embedded DSP functions that offset digital processing burden, often shifting the optimum toward higher sampling rates with relaxed analog filtering.

We now present an example that uses Silanna's SD1148-65 dual ADC in a direct conversion receiver. The RF signal is a 26 MHz-wide band centered at 915 MHz. After downconversion, the baseband I and Q signals extend from 0 to 13 MHz. The ADC sampling rate is set to 65 MS/s. This provides a relaxed anti-alias filter transition band from 13 MHz to 52 MHz.

As shown in Figure 2, SD1148 DSP block offers adders and multipliers that can be programmed to correct the DC offset and IQ gain mismatch. Hardware for IQ phase correction is also present. The user needs to provide control values for these blocks.

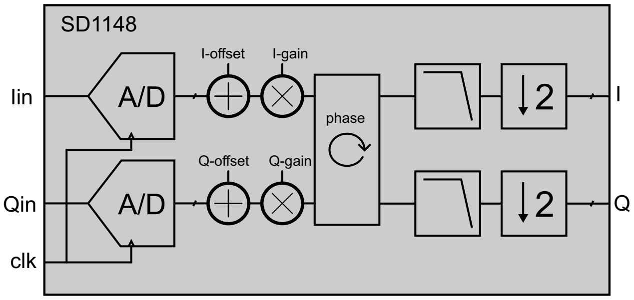

Figure 2. SD1148 configuration for direct conversion receiver application.

The DSP block includes a decimator that can be programmed for rates of two and four. In this case, the rate is set to two. The decimation process includes a digital FIR low-pass filter. Its passband is 40% of the output sampling rate, which in this case is 0.4 × 65 MHz/2 = 13 MHz, matching the requirement. When a low-pass filter is applied to the I and Q paths separately, the combined effect produces a symmetric band-pass response centered at 0 Hz, resulting in a passband from −13 MHz to +13 MHz. Figure 3 shows the frequency-domain signals at each step of this direct conversion receive chain.

The decimator has reduced the output sampling rate to 32.5 MS/s. The combination of oversampling and digital filtering improves the signal-to-noise ratio by about 3 dB for every decimation factor of two.

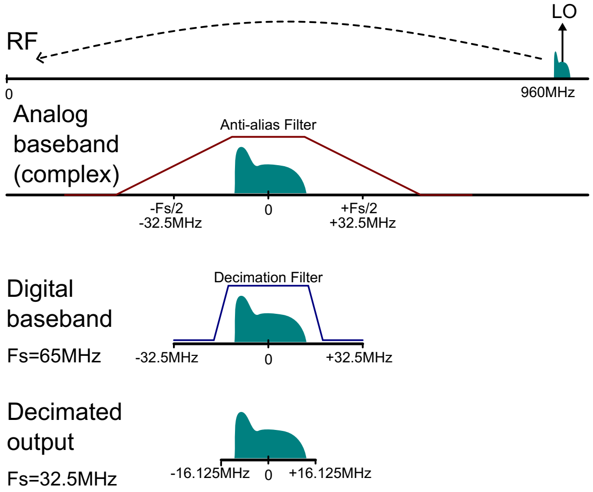

Figure 3. Frequency domain signals in direct conversion receiver.

One thing worth noting is that as the decimation filter suppresses signals in its stop band, the gain control loop of the system can be affected. If a strong signal is present in the ADC input, but filtered out from the digital output, a loop that monitors the output might not detect when the ADC starts to clip. This can be avoided by incorporating the overrange bit provided by the ADC into the gain control algorithm.

Table 1 compares an implementation based on the SD1148 against an implementation using a traditional ADC without DSP features. With a modest increase in sampling rate, the anti-alias filter transition band widens by a factor of 2.8, the SNR improves by 2.1 dB due to oversampling gain, and the output data rate is reduced by 19%.

Additionally, the signal has already been filtered to the final bandwidth, which offloads that processing task from the FPGA.

Table 1.SD1148 compared against a traditional ADC part.

	Traditional ADC part	**SD1148**
ADC sampling rate	40MS/s	65MS/s
Anti-alias filter transition band	14MHz	39MHz
Over sampling gain	1.9dB	4.0dB
Output sampling rate	40MS/s	32.5MS/s

Direct Conversion Receiver with Digital Channel Selection

In our second example, we operate on the same 26MHz RF band, which is further divided into four 6.5MHz channels. The application receives one channel at a time occasionally switching between channels.

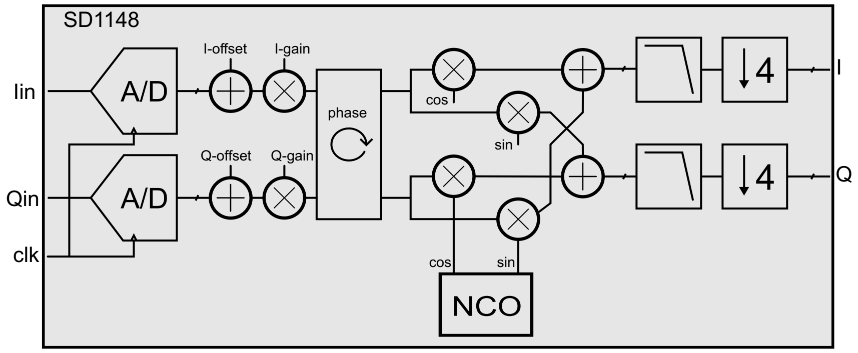

Figure 4. SD1148 useing the built-in DDC to perform channel selection within the digitized band.

The RF and analog portion of the receiver remain the same as in the first example. We enable the digital downconverter (DDC), built into the SD1148 as shown in Figure 4, and tune the numerically controlled oscillator (NCO)—which provides the digital LO—to the center frequency of the desired channel. This shifts the selected channel to 0 Hz, as shown in Figure 5. The decimation factor can then be programmed to four, reducing the output sampling rate to 16.25 MS/s. We can also consider reducing the ADC sampling rate from 65 MS/s to the 50–55 MS/s range, which maintains reasonable anti-alias filter requirements while further reducing output data rate. Using these DSP blocks offloads a significant amount of digital signal processing from the FPGA to the ADC, providing both cost and power savings.

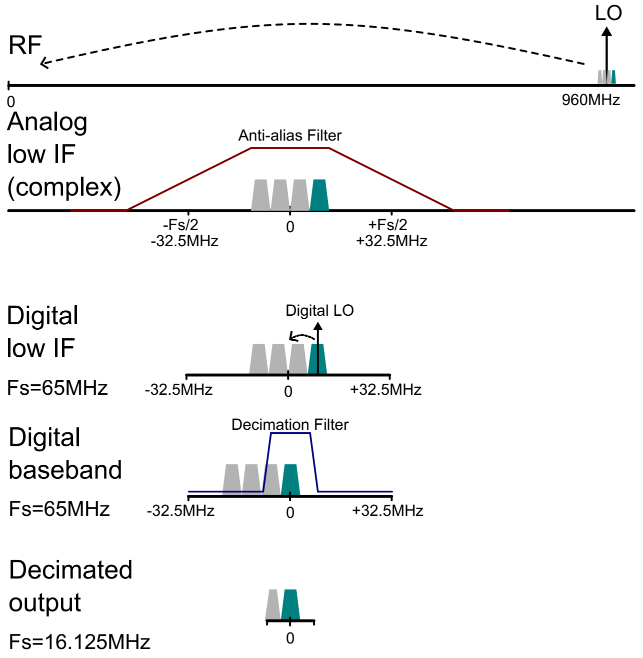

Figure 5. Frequency domain signals in a direct conversion receiver using digital channel selection within the digitized band.

IF Sampling Receiver

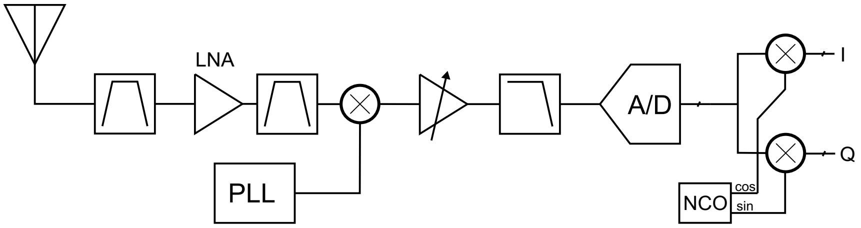

Figure 5. Simplified IF sampling receiver.

The third example uses an IF sampling radio architecture, which is essentially a superheterodyne receiver where the second downconversion stage is implemented digitally. A simplified block diagram of an IF sampling receiver is shown in Figure 6. The RF signal is converted to baseband in two steps: first to an IF where it is digitized, and then to baseband using a digital mixer. This architecture eliminates the issues with IQ matching and the challenges in the vicinity of DC associated with direct conversion receivers. This improvement comes at a cost: the system must address image rejection, which typically requires more analog filtering. In addition, the ADC input is at a higher frequency, which demands a higher-performance ADC and places tighter requirements on sampling-clock jitter. A common way to keep the ADC sampling rate reasonable is to locate the input signal in the second (or third) Nyquist zone. In the IF sampling receiver, the ADC input signal is real, requiring only a single ADC per receive chain instead of a dual-channel device.

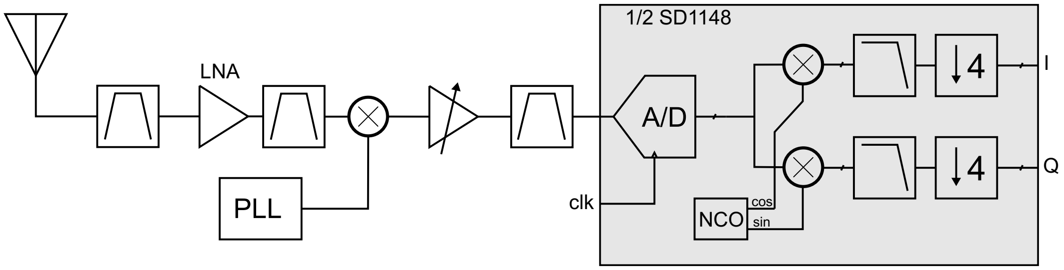

Figure 6. IF sampling receiver uses SD1148 with its DDC and decimation functions enabled.

In this example, we use the SD1148-210 and process a 40 MHz RF signal in the 2.4 GHz ISM band. The IF is chosen as 150 MHz, which places the image 300 MHz away from the desired signal at RF. The ADC sampling rate is chosen as 200 MS/s, which centers the IF in the second Nyquist zone. Operating in higher Nyquist zones requires band-pass anti-alias filtering. In this case, the lower stopband is from DC to 70 MHz, the passband is from 130 MHz to 170 MHz, and the upper stopband is from 230 MHz and above.

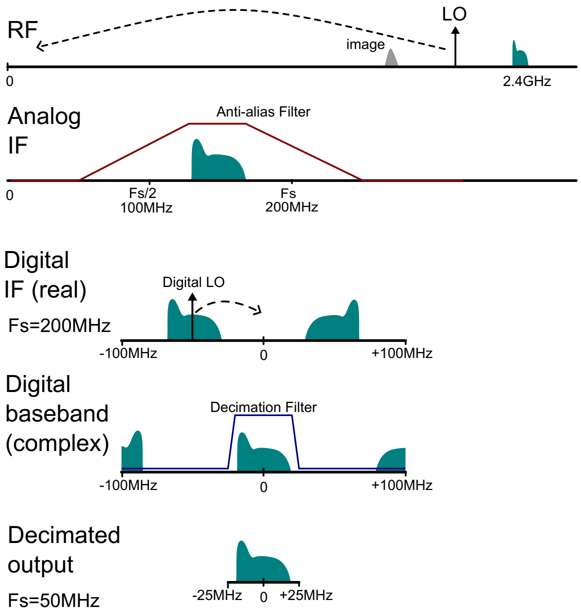

Figure 7. Frequency domain signals in IF sampling receiver.

The aliasing effect—which in this case is a useful feature of the sampling process—is utilized to bring the signal to a 50 MHz center frequency. It is worth noting that the spectrum of a signal originating in the first Nyquist zone appears flipped after sampling. Figure 8 shows the spectrum of the signal throughout the signal chain. Typically, negative frequencies are omitted when dealing with real signals, as they are a mirror image of the positive frequencies. However, it is useful to note that the signal image in the negative frequencies is not flipped relative to the original analog signal. With this insight, we can enable the DDC and program the digital LO to −50 MHz. This rotates the spectrum by 50 MHz toward the positive frequencies, bringing the band to 0 Hz center frequency with the proper orientation. The image originally in the positive frequencies is now shifted toward Fs/2, partially appearing in the negative frequencies around −Fs/2. To remove this unwanted image and reduce excess bandwidth, the decimator must be enabled with a decimation factor of two or more. The 40 MHz signal bandwidth permits additional decimation; therefore, the decimator is set to decimate-by-four. This reduces the output sampling rate to 50 MS/s. Because we have translated a real signal into a complex one, we now have both I and Q components, which together produce the same output rate as a real 100 MS/s signal. The 40% decimator filter bandwidth results in a passband from −20 MHz to +20 MHz, which is a good fit for the 40 MHz signal band.

Conclusion

These three examples demonstrate how the SD1148 DSP features can be applied across different radio architectures to improve performance while reducing system cost and power.

Revision History

Version	Date	Comment
1.0	Apr. 22, 2026	Initial Release.