Application Note: PCB Design Considerations

This application note describes recommended PCB design practices for Silanna's Plural™ ADC product family and focuses on three key PCB design areas:

- Power and ground plane
- Power supply decoupling
- Signal routing

1. Introduction

A printed circuit board (PCB) mechanically supports and electrically connects components using copper traces on an insulating material such as FR-4. PCBs are fundamental to modern electronics and enable compact, high-volume manufacturing.

Multilayer routing and controlled trace geometry allow high-speed signal integrity, but proper layout is especially critical for high-frequency ADC designs. Therefore, the PCB manufacturer's capabilities, such as layer count, trace width, via rules, and minimum pad sizes, must be understood before starting the layout.

2. Power and Ground Plane

Power and ground planes are dedicated copper layers in a multilayer PCB that provide a low-impedance reference and supply voltage distribution across the entire board. Unlike routed traces, planes cover broad areas, giving every component immediate access to supply and return paths. Placing the ground plane immediately adjacent to a power plane creates a distributed capacitance between the two. This passively filters high-frequency noise without any additional discrete components.

The ground plane is the electromagnetic foundation of the PCB and should be implemented as a continuous, uninterrupted layer whenever possible. Splits, slots, and cutouts disrupt return current flow, forcing currents to detour around the discontinuity and creating large loop areas that increase crosstalk and radiated emissions, Figure 1(a).

Figure 1: Plane Splitting. (a)

For every signal current flowing in a trace, an equal and opposite return current flows in the reference plane, as required by Kirchhoff's current law applied to the transmission-line loop. At high frequencies, this return current follows the path of minimum inductance, which lies directly beneath the signal trace. A solid, continuous reference plane, Figure 1(b), ensures a low-inductance return path by tightly coupling the signal and return currents, minimizing loop area and reducing EMI and crosstalk.

When a high-speed signal crosses a slot, gap, or split in its reference plane, the return current is forced to detour around the discontinuity. This detour increases loop area, raises loop inductance, and results in significantly higher radiated emissions and crosstalk. As a rule of thumb, the added inductance is approximately 2nH per centimeter of return-current detour at typical PCB plane thicknesses.

Therefore:

- Never route high-speed traces across plane splits or voids if it can be avoided.
    - If unavoidable, provide a local high-frequency return path by placing a low-ESL stitching/bridging capacitor (for example, a 100nF) immediately adjacent to the crossing on each side of the split.
- Maintaining tight coupling between the signal trace and a continuous reference plane is one of the most effective techniques for controlling return currents and minimizing EMI. Keep analog and digital circuits in separate board zones. Rather than splitting the ground plane, keep the digital and analog components physically separated. Return currents naturally stay within their region without needing a physical barrier.

The ground plane is also the thermal backbone of the PCB. The Plural^{TM} family of ADCs have a large, exposed pad on the bottom side of the package for both grounding and heat dissipation. This pad should be replicated on every board layer and stitched together with a dense array of vias, creating a low inductance return path and an effective thermal conduit. Leaving the thermal pad floating or using too few vias will cause poor heat dissipation and a high-inductance current return path.

3. Power Supply Decoupling

Analog-to-digital converters are highly sensitive to noise on their power supply rails, where even millivolt-level ripple can corrupt conversion results and degrade key performance metrics such as SNDR and SFDR. High-frequency noise is commonly injected onto the power distribution network by switching logic, digital outputs, and neighboring circuitry. In addition, parasitic inductance in PCB power traces may limit the ability to deliver fast transient currents, leading to brief voltage droop at the ADC supply pins.

Decoupling capacitors placed close to the ADC power pins act as local charge reservoirs, providing instantaneous current during transient events. However, a single capacitor is only effective over a narrow frequency range (near the self-resonant frequency), beyond which it exhibits inductive behavior and loses its noise-suppression capability.

As a rule, for choosing decoupling capacitors, once the capacitance value is determined, choose the smallest package available. Alternatively, when a specific package size must be used, choose the highest capacitance value available in that package.

As shown in Figure 2, at low frequencies, the impedance of a decoupling capacitor can be reduced by increasing its capacitance value. At high frequencies, impedance is primarily limited by the capacitor’s parasitic inductance, which must be minimized. While higher capacitance values can often be selected within a given package size, the parasitic inductance of a single, fixed-package capacitor cannot be significantly reduced.

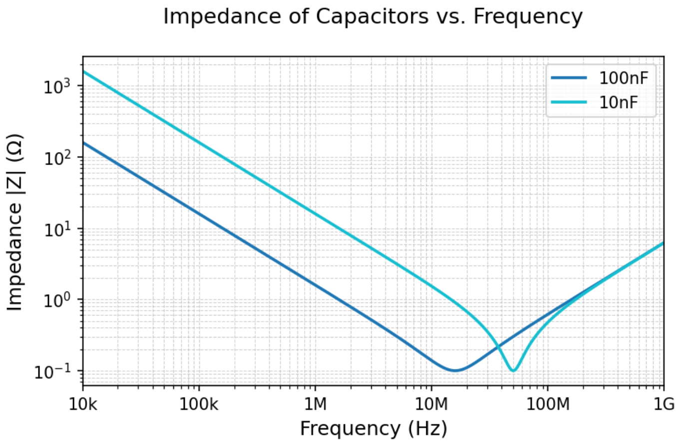

Figure 2: Effect of Package.

To effectively lower inductance, multiple capacitors can be placed in parallel. Parallel capacitors divide the effective parasitic inductance while simultaneously increasing the total capacitance. As a result, both low-frequency and high-frequency impedance are reduced, providing improved decoupling performance across a wider frequency range, as shown by the dashed line in Figure 3.

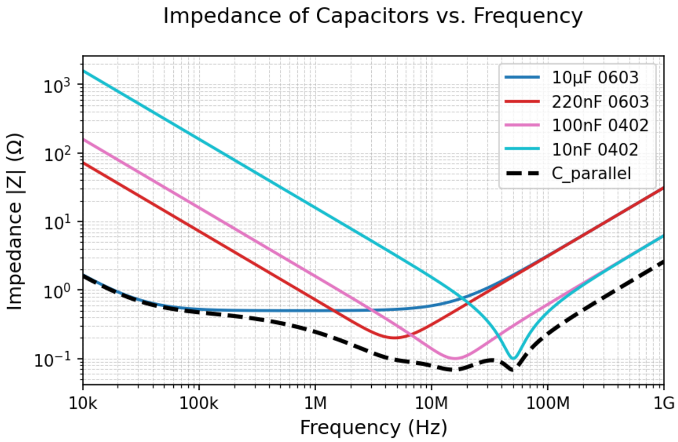

Figure 3: Effect of parallel capacitors, using different size packages.

Finally, place the smallest-value capacitors as close as possible to the IC power pins to reduce trace inductance. Connect each capacitor pad to the ground plane using the shortest trace permitted by the manufacturer's DRC rules and size the trace width to match the capacitor pad to further minimize inductance. If possible, do not share a single ground via with multiple capacitors.

4. Signal Routing

At low frequencies, a PCB trace behaves like a resistor. As switching speeds increase, the electromagnetic wave travelling along the trace takes a non-negligible time to reach the far end. If the driver's transition completes before the wave has travelled to the load and back, reflected waves create ringing, overshoots, and timing skew. This is the transmission line regime.

A trace must be treated as a transmission line when its one-way propagation delay exceeds one-sixth of the signal's rise time:

$$l_{crit} = \frac{t_r}{6 \times t_{pd}}$$

where l_{crit} is the critical length, t_r is the 10-90% transition time (the minimum between the rise and fall time), and t_{pd} is the propagation delay per unit length of the trace. For a microstrip on an FR4 substrate, the propagation delay is about 6ps/mm.

Signals above about 150MHz should not be driven as CMOS; use LVDS instead (e.g. a 250MHz ADC sample clock must be LVDS, not CMOS). Any LVDS trace beyond a few millimeters on FR4 must be impedance-controlled and terminated. The following shows some practical critical lengths for a microstrip on FR4:

Table 1: Critical Length.

Signal Type	Typical Transition Time	Critical Length
CMOS	1.5ns	42mm
LVDS	250ps	7mm

Generally, when possible, keep the traces as short as possible. Avoid vias, as each via adds undesired inductance. No 90° corners, as each corner adds excess capacitance and is an impedance discontinuity (use two 45° bends instead). Any imbalance in length, spacing, or environment can convert into common-mode noise and increase EMI susceptibility.

4.1. Analog Input Network

Even with a perfect ADC, the network that connects the signal source to the ADC input must be able to preserve the signal quality. Figure 4 shows the input network for the Plural^{TM} family of ADCs used in the EVK.

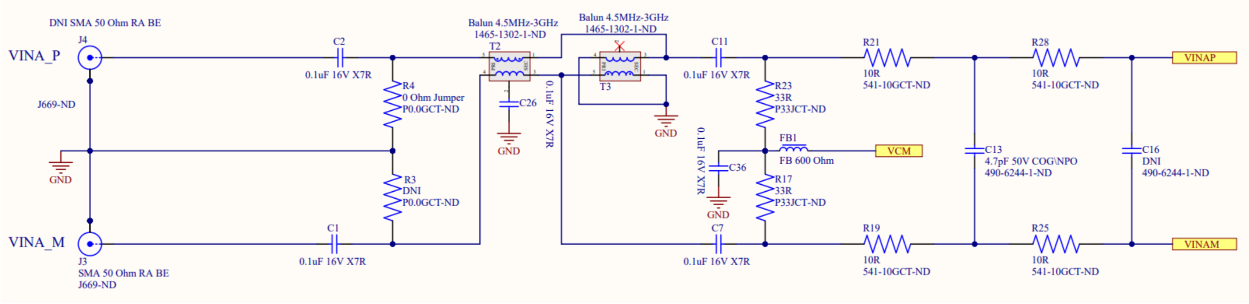

Figure 4: ADC Input Network.

In Figure 4, capacitors C_1, C_2, C_7, and C_{11}, typically 100nF are used to block any DC current into the balun T_2, and T_3, thus preventing core saturation (improving harmonic distortion). If the input is already differential, these components are not required, except for C_7 and C_{11}, when AC-coupling is preferred.

Capacitor C_{36}, R_{17} and R_{23}, provide the common-mode bias from the VCM pin of the ADC through a low-Q choke. C_{36} provides an AC current path for even order harmonics. The PCB layout of this network should be symmetrical with respect to the ADC inputs.

R_{19}, R_{21}, R_{25}, R_{28}, C_{13}, and C_{16} enable the design of various matching networks. Alternatively, R_{21}/R_{28}, and R_{19}/R_{25} could be combined (or replaced by low-Q inductors for higher bandwidth) and are used to prevent any charge kick-back from the ADC input to reach the ADC driver.

Even with a perfect schematic that simulates well with ideal components, the PCB layout is a major source of mismatch. Take the time to keep the layout symmetrical, especially regarding the baluns.

4.2. Clock Network

Similar considerations as for the input network apply to the clock network. Figure 5 shows the input clock network for the Plural^{TM} family of ADCs used in the EVK, excluding the optional crystal oscillator option. In the figure, both the single-ended and differential input options are shown. The schematic can be simplified to fit the clock source.

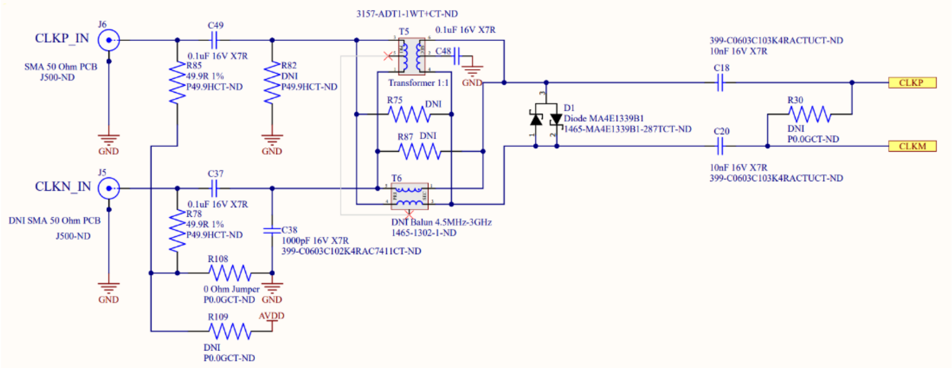

Figure 5: Clock Input Network.

The same PCB layout considerations apply to the input clock network as to the analog input network with one caveat: any signal coupling to the clock could be converted into clock jitter, directly affecting ADC performance.

Use a solid ground reference and keep the analog input and any digital switching signals as far away as possible. Keep differential pairs matched in length and impedance to maintain phase accuracy.

4.3. Digital Output Signals

The digital outputs of the ADC might have to travel a long distance before reaching their destination, such as an FPGA or a microcontroller. In this case, the data wires, especially for high sampling rates, might have to be treated as transmission lines.

A differential pair achieves its 100Ω target through mutual coupling between the two conductors. The stronger the coupling (smaller gap between traces), the lower the odd-mode impedance. The gap-to-width ratio controls Z_{diff}. Rule of thumb (edge-coupled microstrip on FR4 substrate):

- Gap ≤ 2 × trace width (well-coupled differential pair), $Z_{diff} \approx 100\ \Omega$
- Gap > 5 × trace width (weakly coupled), approaches $2 \times Z_{0,single}$

where $Z_{0,single}$ is the characteristic impedance of one trace in isolation.

Maintain a consistent gap throughout the length of the pair. Any taper or pinch introduces a local impedance discontinuity.

Timing skew between D+ and D– translates directly to jitter and eye closure at the receiver. For a 100Mbps data rate, the signal pair should have less than 17mm length mismatch for 100ps maximum skew. An intra-pair skew of less than 20% of the unit interval is generally recommended. When correcting intra-pair length mismatch with serpentines:

- Keep serpentine amplitude less than 3 times the trace width (to avoid coupling the serpentine back into the forward path)
- Place the correction serpentine at the beginning of the route, not at the end (reduces accumulated skew along the route)

Revision History

Version	Date	Comment
1.0	April. 15, 2026	Initial Release.