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Plural ADC
APP-NOTE #105

Application Note: Understanding ADC Parameters

This application note describes ADC parameters used in the specification of the DC and AC performance metrics in the datasheets for the Plural™ family of ADC products. This application note is only a reference.

Introduction

An analog-to-digital converter (ADC) maps a continuous analog input voltage to a discrete digital code. In an ideal N-bit converter the transfer function is a perfectly uniform staircase: each of the 2^N output codes spans exactly one least-significant bit (LSB), the transitions are evenly spaced across the full-scale range, and the converter introduces no noise beyond the unavoidable ±½ LSB quantization error.

Real converters deviate from this ideal in two distinct ways:

- **DC (static) errors**: imperfections in the shape of the transfer function that are present even with a slow-moving or constant input. These include gain error, offset error, differential non-linearity (DNL), and integral non-linearity (INL).
- **AC (dynamic) errors**: imperfections that manifest only when the input is changing, and whose severity typically worsens with input frequency. These include signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), total harmonic distortion (THD), intermodulation distortion (IM3/IMD), and effective number of bits (ENOB).

Both categories appear in any ADC datasheet, and both matter, but for different reasons and in different applications. A clear understanding of how these parameters influence system performance is essential to selecting the right converter, integrating it successfully, and avoiding unexpected performance limitations at the system level.

Datasheet parameters are not abstract figures of merit; each one maps directly to a measurable effect in a real system. A system designer who understands these parameters can:

- Select the right converter: matching datasheet specifications to the application's actual requirements rather than defaulting to the highest resolution or fastest sample rate.
- Budget system-level performance: cascading noise and distortion from the signal source through the anti-alias filter, the Plural™ ADC, and the digital back-end to predict overall dynamic range.
- Identify the dominant limitation: whether performance is being lost to quantization, thermal noise, reference noise, aperture jitter, input driver distortion, or PCB layout.
- Interpret measurement results: recognizing when a bench measurement differs from the datasheet value, and diagnosing whether the cause is the converter, the test circuit, or the measurement method.

DC Parameters

DC parameters describe the accuracy of an ADC's transfer function under static or quasi-static conditions. They are measured by sweeping a slowly varying (or stepped) input across the full-scale range and comparing each output code transition to its ideal position. All definitions below follow IEEE Std 1241-2010, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters.

LSB Size

The least-significant bit (LSB) is the foundational unit against which all DC errors are expressed. For an N-bit ADC with full-scale range (FSR): 1 LSB = FSR / 2^N, referred to the ADC input. All DNL and INL figures in a datasheet are dimensionless multiples of this LSB value.

Offset Error

The Plural ADCs use a differential input stage. The input range spans both positive and negative voltages (differentially). The offset error is the deviation of the actual mid-scale transition from its ideal position, expressed in %FSR.

Offset error = $V_{actual\_midscale\_transition} - V_{ideal\_midscale\_transition}$

A fixed offset shifts every output code by the same amount. In measurement applications this produces constant DC error. In AC applications, it has negligible effect on dynamic performance because the offset falls outside the signal band.

Gain Error

The gain error is the deviation of the actual full-scale span from the ideal full-scale span, expressed as a percentage of full scale or in LSBs.

Gain error = $(V_{actual\_last\_transition} - V_{actual\_first\_transition}) - (V_{ideal\_last\_transition} - V_{ideal\_first\_transition})$

Gain error scales linearly with signal amplitude. It is equivalent to a multiplier error on the input. At ±1% gain error, a signal nominally at 80% of full-scale spans either 79.2% or 80.8%. In precision measurement this limits absolute accuracy; in AC applications it affects amplitude calibration but not dynamic range directly.

When both offset and gain errors are present, the ADC's transfer function is shifted and scaled from the ideal. The sum of offset and gain errors is sometimes referred to as full-scale error.

Offset and Gain Error Mismatch

In Plural™ ADC devices that contain two or more converter channels sharing a package, mismatch is the difference in offset error or gain error between the two channels, measured under identical conditions, as percent of the FSR:

Offset mismatch = $\text{Offset}_{channel\_A} - \text{Offset}_{\_channel\_B}$

Gain mismatch = $\text{GainError}_{channel\_A} - \text{GainError}_{channel\_B}$

Mismatch is distinct from the absolute error of any individual channel. Each channel may be trimmed to reduce its own absolute offset and gain, but process gradients across the die mean that the trim residuals differ between channels.

In systems that use multiple ADC channels for simultaneous sampling, such as phased-array radar, multi-channel oscilloscopes, I/Q demodulators, multi-axis motion control, channel mismatch creates correlated errors that cannot be removed by a single system-level calibration constant:

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Commented [MW1]: This sounds a little bit a LSB definition for a DAC or ADC LSB referred to the input. ADC user is mostly interested in the digital output, where the LSB is 1.

Commented [CP1R2]: Maybe. That's what I am used to. The definition is still correct as the LSB is the FSR/2^NBIT. Isn't it?

Commented [MW2]: This sounds like the offset definition for single-ended ADCs. I think it should be defined around the mid-code.

- Offset mismatch produces a DC difference between channels. In an I/Q receiver this appears as LO feed-through and degrades image rejection. In a phased-array system it introduces a channel-to-channel phase bias that degrades beam-forming accuracy.
- Gain mismatch between channels causes amplitude imbalance. In an I/Q system this directly degrades image rejection ratio (IRR):

$\text{IRR (dBc)} \approx -20 \times \log_{10}(\Delta G / 2)$

where ΔG = fractional gain mismatch (e.g. 0.01 for 1% mismatch)

Offset and Gain Error Drift

Offset and Gain Error Drift are the change in offset error or gain error per unit change in temperature, expressed in ppm of full scale per °C (ppm/°C) in the Plural ADCs datasheets.

Differential Non-Linearity

Differential Non-Linearity (DNL) is the deviation of any single code width from the ideal width of 1 LSB, expressed in LSBs:

$\text{DNL}(k) = \text{code}(k) - 1\ \text{LSB}$

For an ideal ADC, DNL = 0 for all codes. If $\text{DNL}(k) \leq -1$ LSB for any code k, that code is never produced regardless of the input. This is a missing code. A converter with DNL > −1 LSB is guaranteed monotonic. DNL ≥ −1 LSB is the necessary and sufficient condition for an ADC to have no missing codes. DNL errors generate harmonic distortion for sine-wave inputs, because unequal code widths create periodic errors in the output.

Integral Non-Linearity

Integral Non-Linearity (INL) is the deviation of the actual transfer function from a best-fit (or end-point) straight line at any code transition, expressed in LSBs:

$\text{INL}(k) = (\text{actual transition voltage of code } k) - (\text{ideal transition voltage from best-fit line})$

INL(k) is also the cumulative sum of all DNL errors:

$\text{INL}(k) = \Sigma\, \text{DNL}(i), \text{ for } i = 1 \text{ to } k$

End-point vs. best-fit: Some datasheets use a line between the first and last transitions (end-point); others use a least-squares best-fit line. Best-fit INL is always less than the end-point INL in magnitude.

INL determines DC measurement accuracy. The shape of the INL is related to the type of dynamic distortion that the ADC exhibits: a second order (bow-shaped) INL produces second harmonic distortion for sinusoidal inputs; an odd-symmetric (S-shaped) INL produces third harmonic distortion. This directly connects the DC spec to SFDR.

AC Parameters

AC parameters characterize how faithfully an ADC reproduces a time-varying signal. They are measured by applying a spectrally pure sinusoidal input at a known frequency and amplitude, digitizing a coherent block of samples, and computing the FFT.

Signal-to-Noise Ratio

Signal-to-Noise Ratio (SNR) is the ratio of the RMS fundamental amplitude to the RMS of all noise components, excluding harmonics and DC:

$SNR = 20 \times \log_{10}(V_{signal\_rms} / V_{noise\_rms})$ [dB]

For an ideal N-bit ADC with a full-scale sine wave input, the theoretical maximum, including quantization noise only, is given by:

$SNR\_ideal = 6.02 \times N + 1.76$ [dB]

A real ADC is affected by other sources of noise, such as:

- Thermal noise
- Aperture jitter
- Reference noise
- Clock phase noise
- Non-precise quantization levels

Thermal noise, a fundamental, unavoidable noise source that exists whenever components with resistance operate at a temperature above absolute zero, is the random voltage or current fluctuation generated by the thermal agitation of charge carriers in the ADC's analog circuitry. It mainly originates from the input sampling network (switch resistance and sampling capacitor), the front-end amplifier or buffer, and the bias resistors and reference circuitry.

Aperture jitter is the random uncertainty in the exact time at which the ADC samples the input signal. Instead of sampling at a perfectly precise instant, the sampling clock exhibits small, random timing variations, causing the input voltage to be measured slightly earlier or later than intended. Because a time error translates into a voltage error when the input signal is changing, aperture jitter effectively converts timing noise into amplitude noise. Its impact increases with the slew rate of the input signal and therefore becomes more severe at higher input frequencies.

Aperture jitter is input-frequency dependent and set an SNR ceiling at:

$SNR_{jitter} = -20 \times \log_{10}(2\pi \times f_{in} \times t_j)$

where f_{in} is the input frequency and t_j is the aperture jitter RMS value.

Reference noise is the unwanted fluctuation in the ADC's reference voltage, which sets the scale against which the input signal is measured. Because every digital code corresponds to a fraction of the reference voltage, any noise or variation on this reference modulates the signal being converted and translates into conversion errors.

Clock phase noise is the short-term, random fluctuation of a clock signal's instantaneous phase around its ideal, perfectly periodic position. It represents timing instability in the frequency domain and is typically specified as single-sideband phase noise, measured in dBc/Hz at a given offset frequency from the carrier.

NOTE: Aperture jitter represents the ADC's own internal contribution to total clock jitter and is a device-specific parameter documented in the datasheet. Clock phase noise, by contrast, is a system-level characteristic that influences the ADC's noise performance but is not intrinsic to the converter itself and therefore is not specified in the ADC datasheet. See "*APP-NOTE #101: Understanding Clock Jitter in High-Speed ADCs*" for a deeper understanding.

Signal-to-Noise-and-Distortion

Signal-to-Noise-and-Distortion (SNDR) is the ratio of the RMS fundamental to the RMS of all other components, noise and harmonics combined:

$$\mathrm{SNDR} = 20 \times \log_{10}(V_{\mathrm{signal\_rms}} / V_{\mathrm{noise+distortion\_rms}})\ [\mathrm{dB}]$$

SNDR is always less than SNR, since it includes the contribution of distortion in the denominator. When harmonic distortion is negligible relative to noise, SNDR is (almost) equal to SNR. SNDR is the basis for ENOB calculation and is often considered the most complete single-number summary of dynamic performance.

The relationship between SNR, THD, and SNDR follows from power addition:

$$1 / \mathrm{SNDR}_{\mathrm{linear}} = 1 / \mathrm{SNR}_{\mathrm{linear}} + 1 / \mathrm{THD}_{\mathrm{linear}}$$

where each term is expressed as a linear power ratio (not dB).

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the RMS sum of harmonic components, generally from the second harmonic through the fifth harmonic, relative to the fundamental:

$$\mathrm{THD} = 20 \times \log_{10}(\sqrt{(H2^2 + H3^2 + H4^2 + H5^2)} / P_{\mathrm{fundamental}})[\mathrm{dB}]$$

The Plural ADCs use a differential input stage and mainly exhibit odd-symmetric non-linearity. THD is typically dominated by the third harmonic component at higher frequencies. As THD can be calculated from the SNR and SNDR, it is generally not reported in the Plural ADC datasheet.

Spurious-Free Dynamic Range

Spurious-Free Dynamic Range (SFDR) is the ratio of the fundamental amplitude to the single largest spurious spectral component, anywhere in the Nyquist band:

$$\mathrm{SFDR} = P_{\mathrm{fundamental}} - P_{\mathrm{worst\_spur}}\ [\mathrm{dBc}]$$

The worst spur may be a harmonic or a non-harmonic spur caused by intermodulation with the clock frequency, power supply ripple, or internal digital switching noise.

Because harmonic and intermodulation products grow faster than the fundamental as input amplitude increases (3:1 slope for third-order terms), SFDR improves when the input is reduced below full scale. As a generally accepted standard, the Plural ADC datasheets specify the SFDR operating at −1dBFS (unless otherwise noted in the datasheet).

Intermodulation Distortion

When two spectrally pure tones at frequencies f_1 and f_2 are applied simultaneously to an ADC input, any non-linearity in the signal path (input driver, sampling network, or converter core) produces additional frequency components that were not present at the input. These are intermodulation products, and they appear at combinations of the input tones: $m \cdot f_1 \pm n \cdot f_2$, where m and n are integers.

In practice, the most troublesome terms are usually the third-order products because they tend to be relatively large and fall close to the desired signals. For a two-tone test, the dominant third-order components occur at $2f_1 - f_2$ and $2f_2 - f_1$. These products often land inside the same band as the desired signal (especially for closely spaced tones), so they cannot be removed with filtering after the ADC and directly limit usable dynamic range in wideband receivers and multi-carrier systems.

IM3 is typically measured with two equal-amplitude tones (often each set -6dB below full scale) and reported in dBc, referenced to the power in either fundamental tone. Lower (more negative) IM3 indicates better linearity.

$IM3 = 10 \times \log_{10}(P_{IM3} / P_{fundamental})$ [dBc]

Effective Number of Bits

Effective Number of Bits (ENOB) expresses SNDR as an equivalent ideal-converter resolution:

$ENOB = (SNDR - 1.76) / 6.02$

This inverts the ideal SNR formula (SNR_ideal = 6.02N + 1.76), giving a single number that encapsulates both noise and distortion performance regardless of the nominal resolution.

ENOB degrades with input frequency because aperture jitter contribution to noise grows as $20 \times \log_{10}(f\_in)$.

The data-converter industry has adopted a practice whereby the ENOB of high-speed ADCs with nominal resolutions above 12 bits is significantly lower than the stated resolution. For example, 14-bit ADCs typically achieve an ENOB in the range of 11.8 to 12.3 bits. The primary reason is that achieving a true 12-bit thermal noise floor is costly in terms of power consumption and silicon area. In pipelined ADC architectures, however, adding additional quantization levels and output bits is relatively inexpensive. As a result, designers include extra bits to suppress quantization noise and allow thermal noise to be the dominant limit on overall ADC performance.

The Plural™ ADC datasheets always include a plot showing how the SNR, SNDR and SFDR change with the input frequency.

References

1. IEEE Std 1241-2010, IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE, 2011.
2. Silanna Semiconductor, Plural ADCs, www.silannasemi.com/plural-adcs, 10-16 bit ADC platform.

Revision History

Version	Date	Comment
1.0	April. 15, 2026	Initial Release.