



## Application Note: SocketSwap, Plural ADC Detection via the Serial Port Interface

### Register Conversion Tool

Silanna provides a web-based conversion tool, **SocketSwap**, which translates register writes from Analog Devices and Texas Instruments devices into the Plural ADC register format. The tool is accessible through the Plural ADC support page <https://silannasemi.com/plural-support/socketswap>.

The Plural ADC register map, including complete register and bit-field descriptions, is fully documented in the device datasheet.

### Plural ADC Detection Introduction

Silanna's customers use Plural ADC parts as pin-to-pin replacements of legacy parts from Analog Devices (ADI) and Texas Instruments (TI) in existing designs. Many applications use SPI to program the ADC control registers. The register map and in some cases the SPI protocol used in Plural ADCs are not always one to one matching with ADI and TI parts. When mixing production volume between Silanna and ADI or TI, the user may need to detect whether the board is populated with a Silanna part or an ADI or TI part. This application note shows a method for achieving that using simple SPI write and read.

### Plural ADC SPI Protocol

The Plural ADCs support a 3-wire Serial Port Interface (SPI) for AD9xxx replacement parts and a 4-wire SPI for both ADC42xx and LTC21xx replacement parts. Both interfaces use the following signals:

- **SCLK** defines the bit rate at which serial data is driven onto, and sampled from, the bus
- **CSB** defines the boundaries of a basic data 'unit', comprised of multiple serial bits

The 3-wire SPI uses:

- **SDIO** as the serial data I/O wire

while the 4-wire interface uses:

- **SDI**: as the serial data input wire
- **SDO**: as the serial data output wire

The read and write cycles are described in Figure 1 and Figure 2.

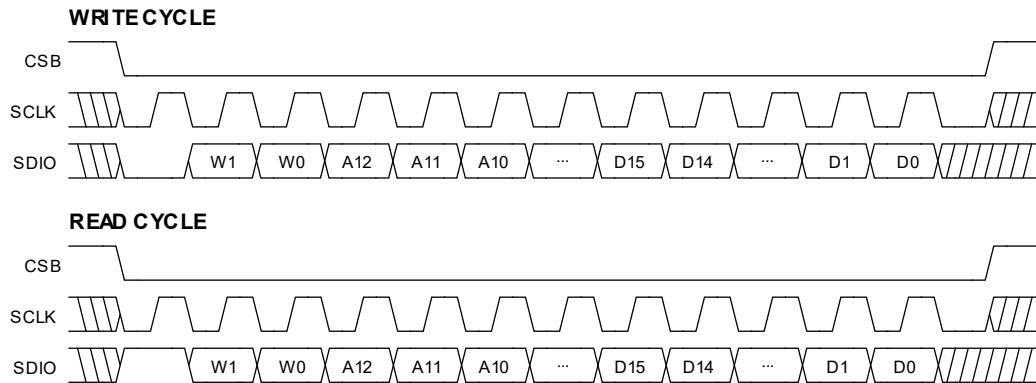


Figure 1: 3-wire SPI.

The falling edge of CSB combined with the rising edge of SCLK marks the start of the transaction. The complete instruction cycle is 32-bits long. The address space is 13 bits long (A<12:0>) and the data is 16 bits wide (D<15:0>). The first bit of the serial word specifies the transfer direction, R/W: a 0 selects a write operation, while a 1 selects a read operation.

Only the read cycle is affected by the SPI interface type.

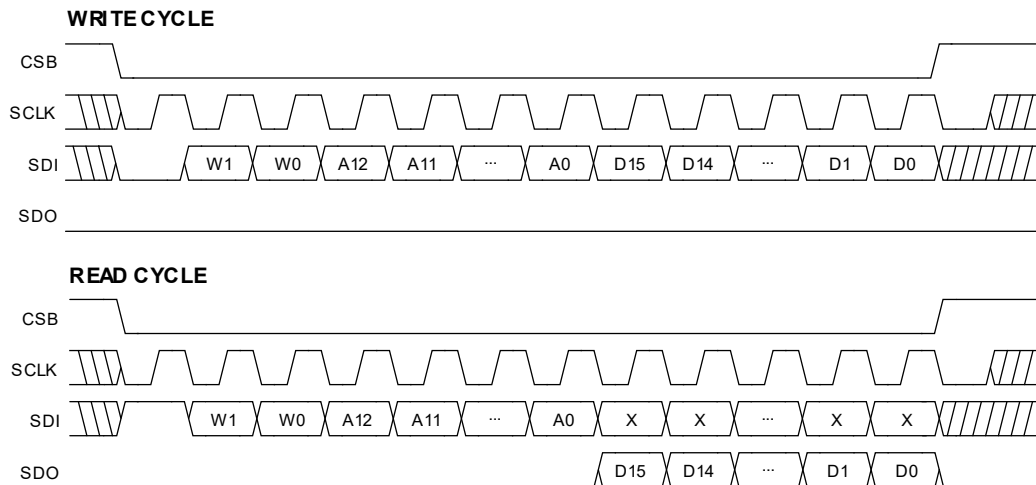


Figure 2: 4-wire SPI.

Two bits, W1 and W0, determine how many bytes of data can be transferred in the same write cycle (see Table 1). If more than 16 bits (2 Bytes) of data are being transferred the address is increased sequentially.

Table 1: SPI Word Length.

[W1, W0]	Data Length
00	Not Supported
01	Two bytes of data can be transferred
10	Not Supported

11

Four bytes of data can be transferred

## Plural Replacement of an ADI AD9xxx Part

Plural ADC SPI protocol is compatible with AD9xxx protocol in two data byte mode (W1, W0 = 0b01). The Plural part does not support one data byte mode (W1, W0 = 0b00).

### Detection Procedure

- AD9xxx part is used in two data byte mode
  - Read register 0x01. If the read back LSB byte value is 0x18, the board is populated with AD9xxx part. If the readback LSB byte value is 0x00, it is populated with Plural ADC part. Plural register map can be used to program the part without protocol changes.
- AD9xxx part is used in one data byte mode
  - Read register 0x00. If the read back value is 0x18, the board is populated with AD9xxx part. If the readback value is 0x00, it is populated with Plural ADC part. Switch to two byte mode and use Plural register map to program the part.

## Plural Replacement of an ADI LTC21xx Part

LTC21xx parts use SPI protocol with 7-bit address and 8-bit data and no W1, W0 bits, which is incompatible with Plural SPI protocol.

### Detection Procedure

Write 0x01 to register 0x04 using LTC21xx SPI protocol. Read back the same register. If the value is 0x01, the board is populated with LTC21xx part. Restore register 0x4 to the default value by writing 0x00 to it. If the read back value is 0x00, the board is populated with Plural ADC part. Switch to the Plural SPI protocol and use the Plural register map to program the part.

## Plural Replacement of a TI ADS42xx Part

ADS42xx parts use SPI protocol with 8-bit address and 8-bit data and no R/W bit nor W1, W0 bits, which is incompatible with the Plural SPI protocol. Readback is enabled by first writing 0x1 to register address 0x00.

### Detection Procedure

Enable readback mode by writing 0x01 to register 0x00 and then read the register 0x00 using ADS42xx SPI protocol. If the readback value is 0xff, the board is populated with ADS42xx part. If the read back value is 0x00, the board is populated with Plural ADC part. Switch to the Plural SPI protocol and use the Plural register map to program the part. Notice that Plural ADC SPI uses the rising clock edge to capture the SPI data.



## Revision History

Version	Date	Comment
1.0	Mar. 3, 2026	Initial Release.

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